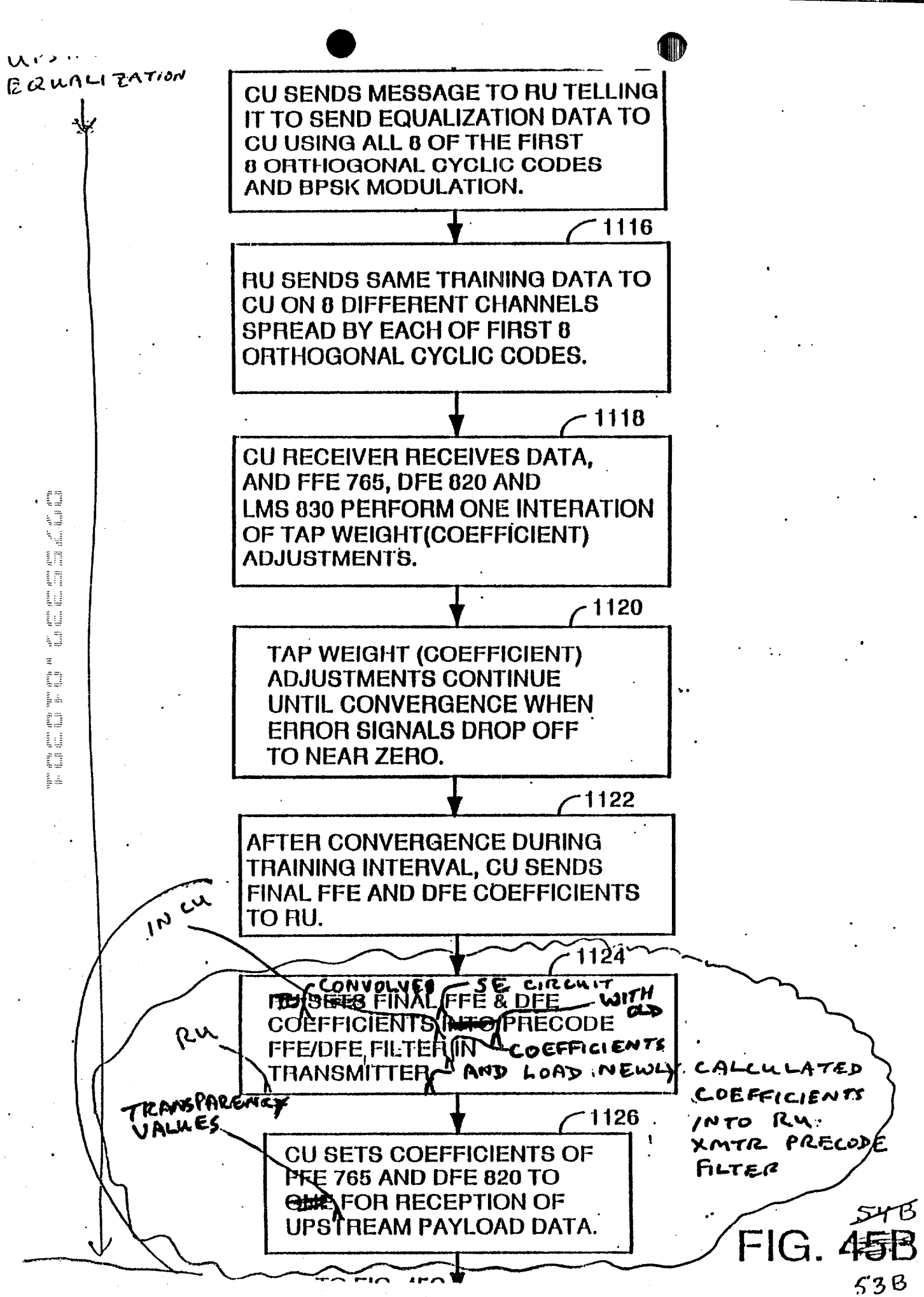

EQUALIZATION
CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.
1116
RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.
1118
CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.
1120
TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.
1122
AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.
IN CU
1124
CU SETS FINAL FFE & DFE COEFFICIENTS INTO PRECODE FFE/DFE FILTER IN TRANSMITTER
CONVOLVE SE CIRCUIT WITH OLD COEFFICIENTS AND LOAD NEWLY CALCULATED COEFFICIENTS INTO RU XMTR PRECODE FILTER
RU
TRANSPARENCY VALUES
1126
CU SETS COEFFICIENTS OF PFE 765 AND DFE 820 TO ONE FOR RECEPTION OF UPSTREAM PAYLOAD DATA.
54B
FIG. 45B
53B

FAXED TO
DI MUELLER
10/25/00
(909) 596-3733

FROM FIG. 45B

DOWNSTREAM EQUALIZATION

1128

CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

1130

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

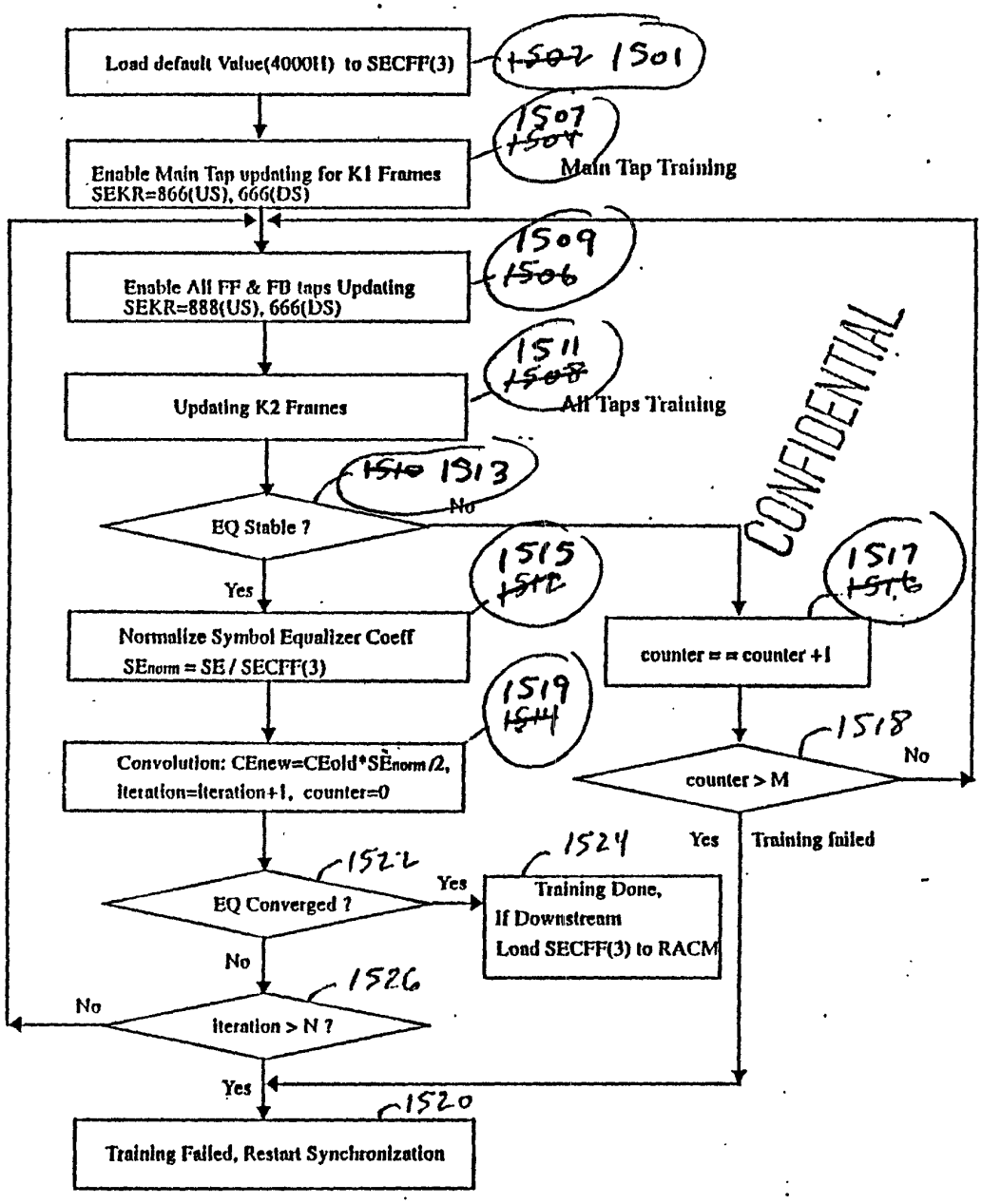
1132

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND ~~LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764~~; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AN DFE FILTERS O CE CIRCUIT 764 AND LOADS THE NEWLY CALCULA ED TAP WEIGHT INTO THE FFE AND DFE FILTERS OF THE CE CIRCU

~~54C~~
FIG. ~~45C~~
53C

Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

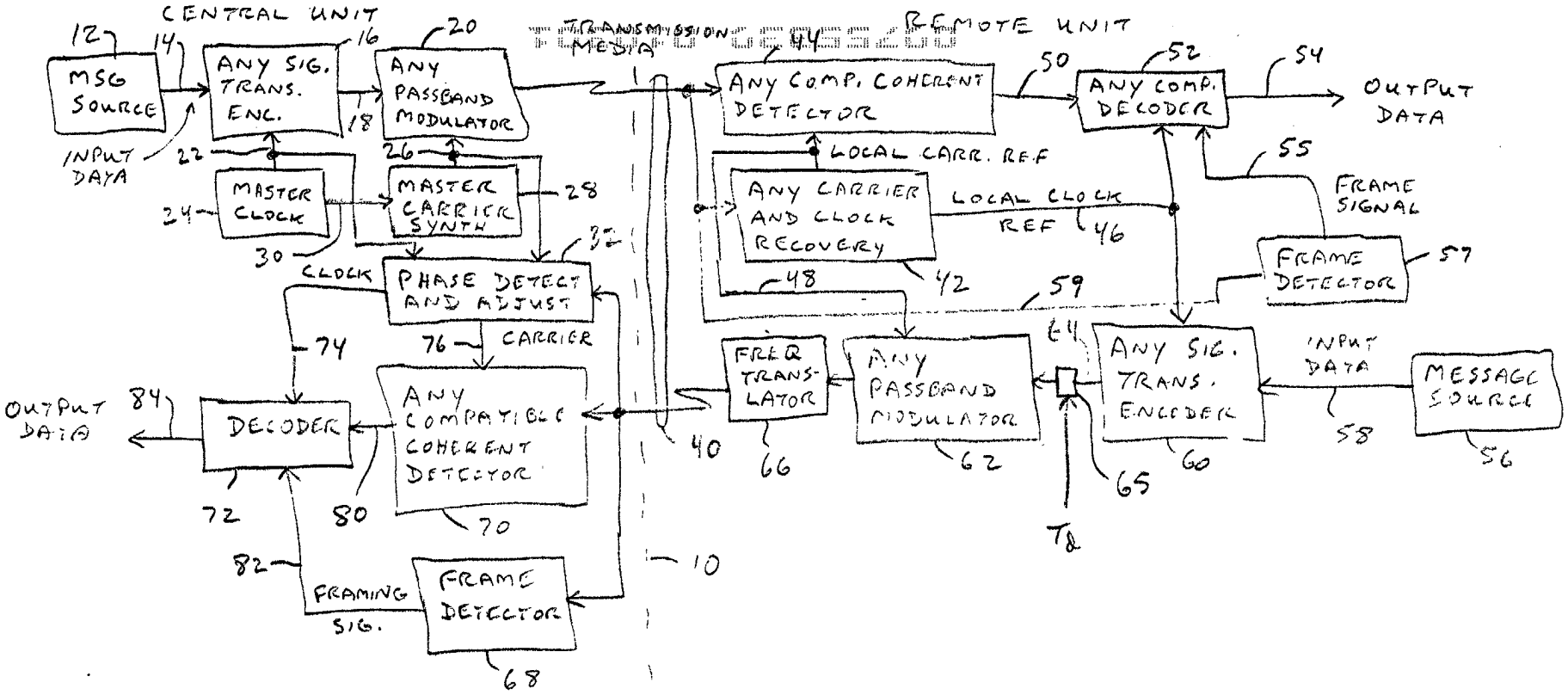

CENTRAL UNIT
REMOTE UNIT
TRANSMISSION MEDIA
MSG SOURCE
ANY SIG. TRANS. ENC.
ANY PASSBAND MODULATOR
INPUT DATA
MASTER CLOCK
MASTER CARRIER SYNTH
CLOCK
PHASE DETECT AND ADJUST
CARRIER
DECODER
OUTPUT DATA
ANY COMPATIBLE COHERENT DETECTOR
FRAMING SIG.
FRAME DETECTOR
ANY COMP. COHERENT DETECTOR
LOCAL CARR. REF
ANY CARRIER AND CLOCK RECOVERY
LOCAL CLOCK REF
FREQ TRANS-LATOR
ANY PASSBAND MODULATOR
ANY COMP. DECODER
OUTPUT DATA
FRAME SIGNAL
FRAME DETECTOR
ANY SIG. TRANS. ENCODER
INPUT DATA
MESSAGE SOURCE
12
14
16
18
20
22
24
26
28
30
32
40
42
44
46
48
50
52
54
55
56
57
58
59
60
62
64
65
66
68
70
72
74
76
80
82
84
10
Td

FIG. 1

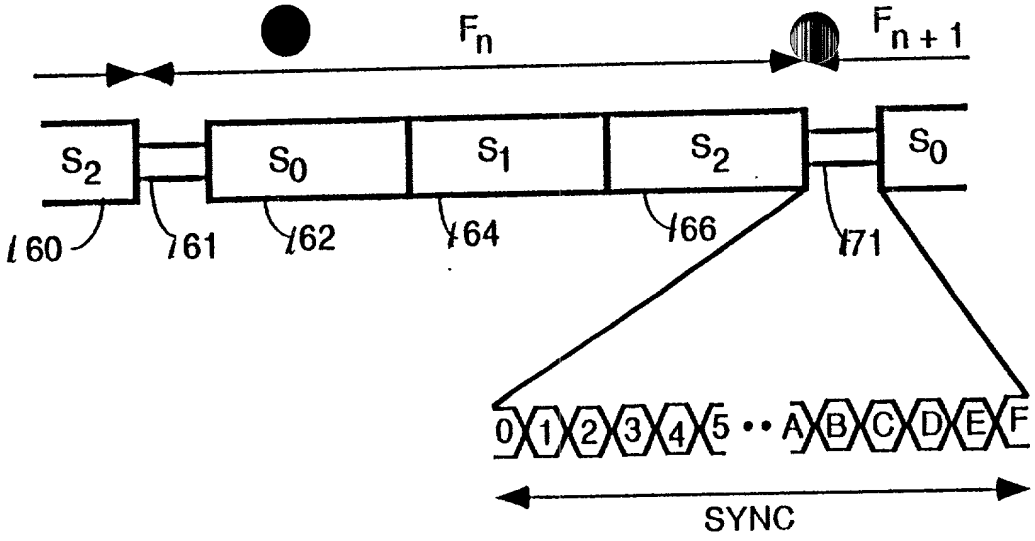

F_n
F_{n+1}
S_2
S_0
S_1
S_2
S_0
160
161
162
164
166
171
0 1 2 3 4 5 • • A B C D E F
SYNC

FIG. 4A

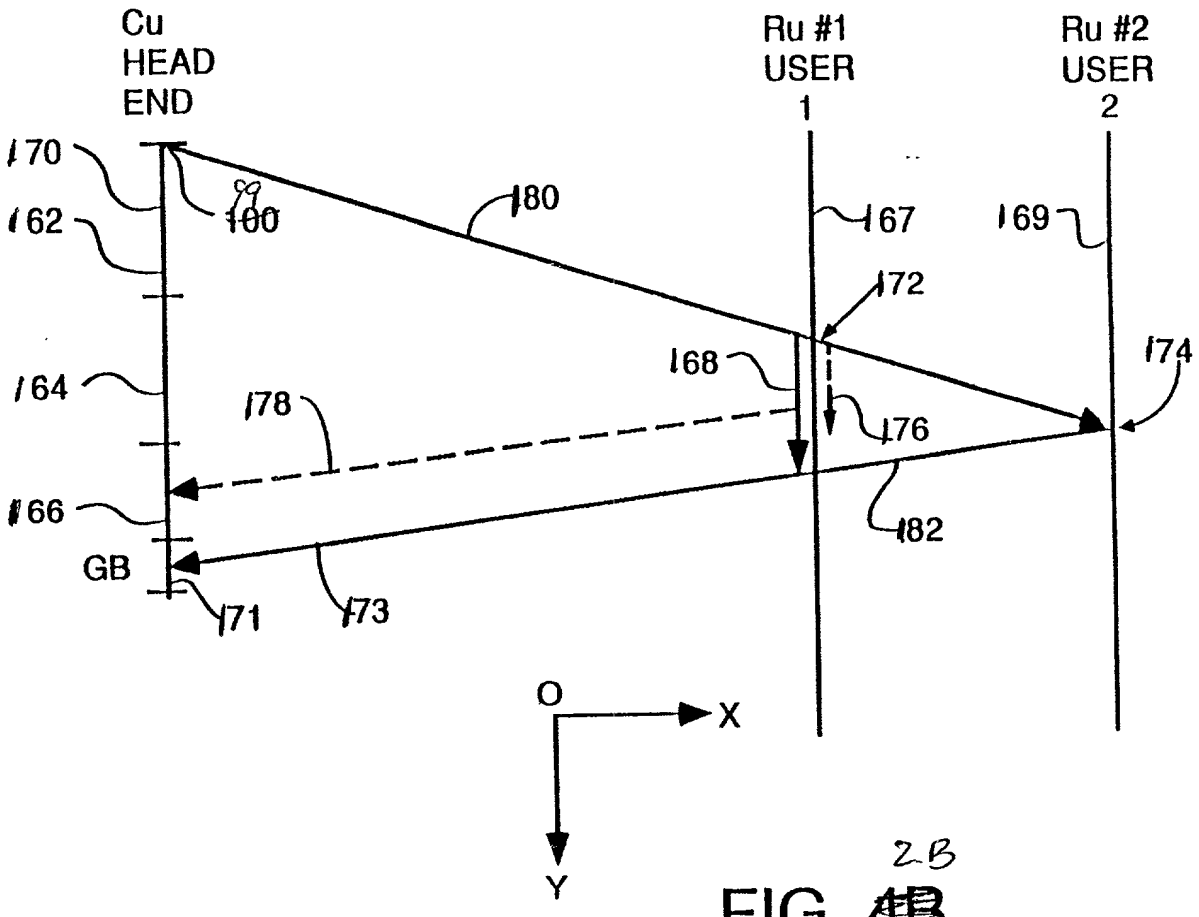

Cu
HEAD
END
Ru #1
USER
1
Ru #2
USER
2
170
162
164
166
GB
171
100
180
167
169
172
168
174
178
176
182
173
O
X
Y

FIG. 4B

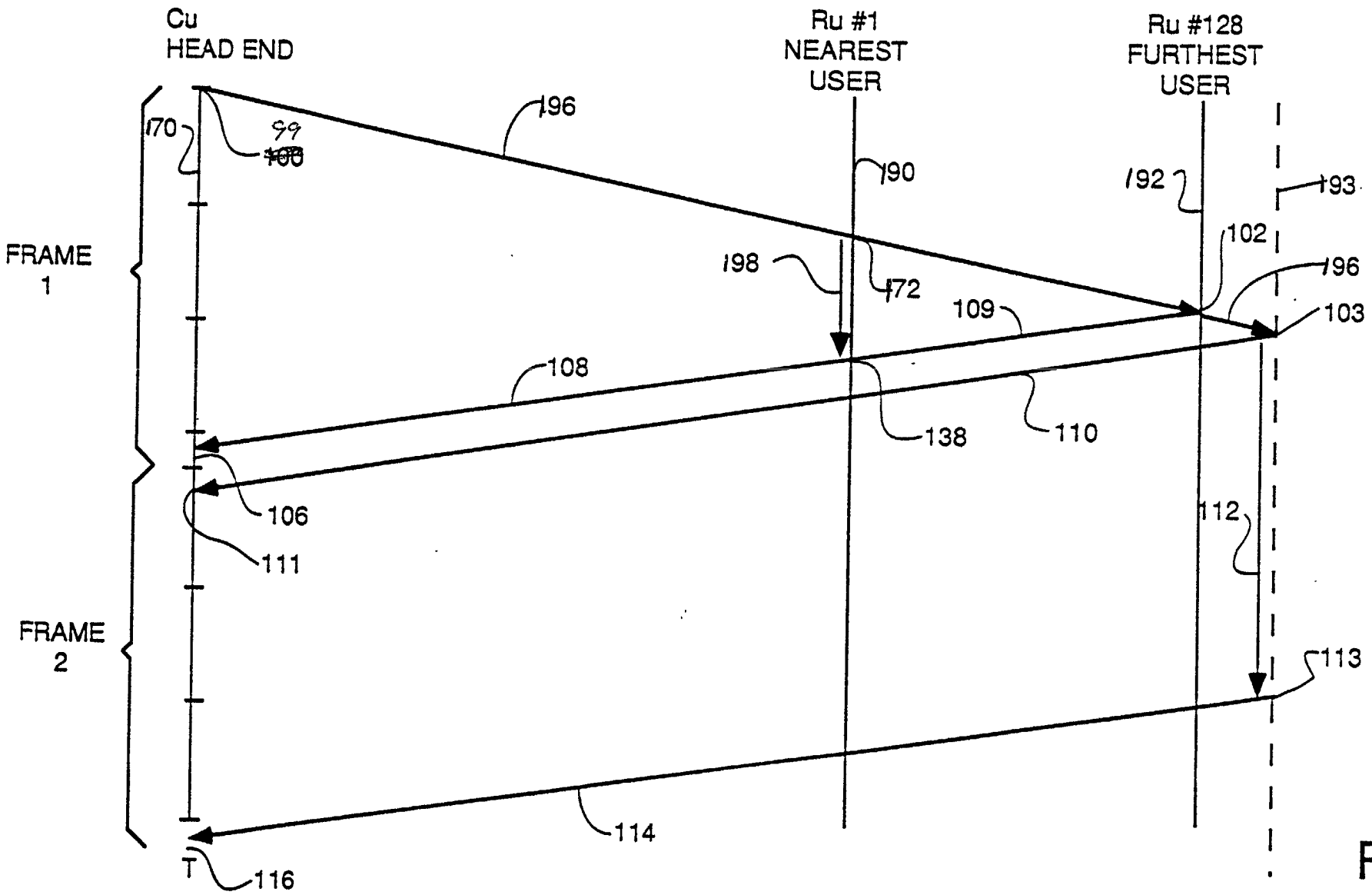

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
1
FRAME
2
170
99
100
196
190
192
193
102
198
172
196
109
103
108
138
110
106
111
112
113
114
T
116

FIG. 5

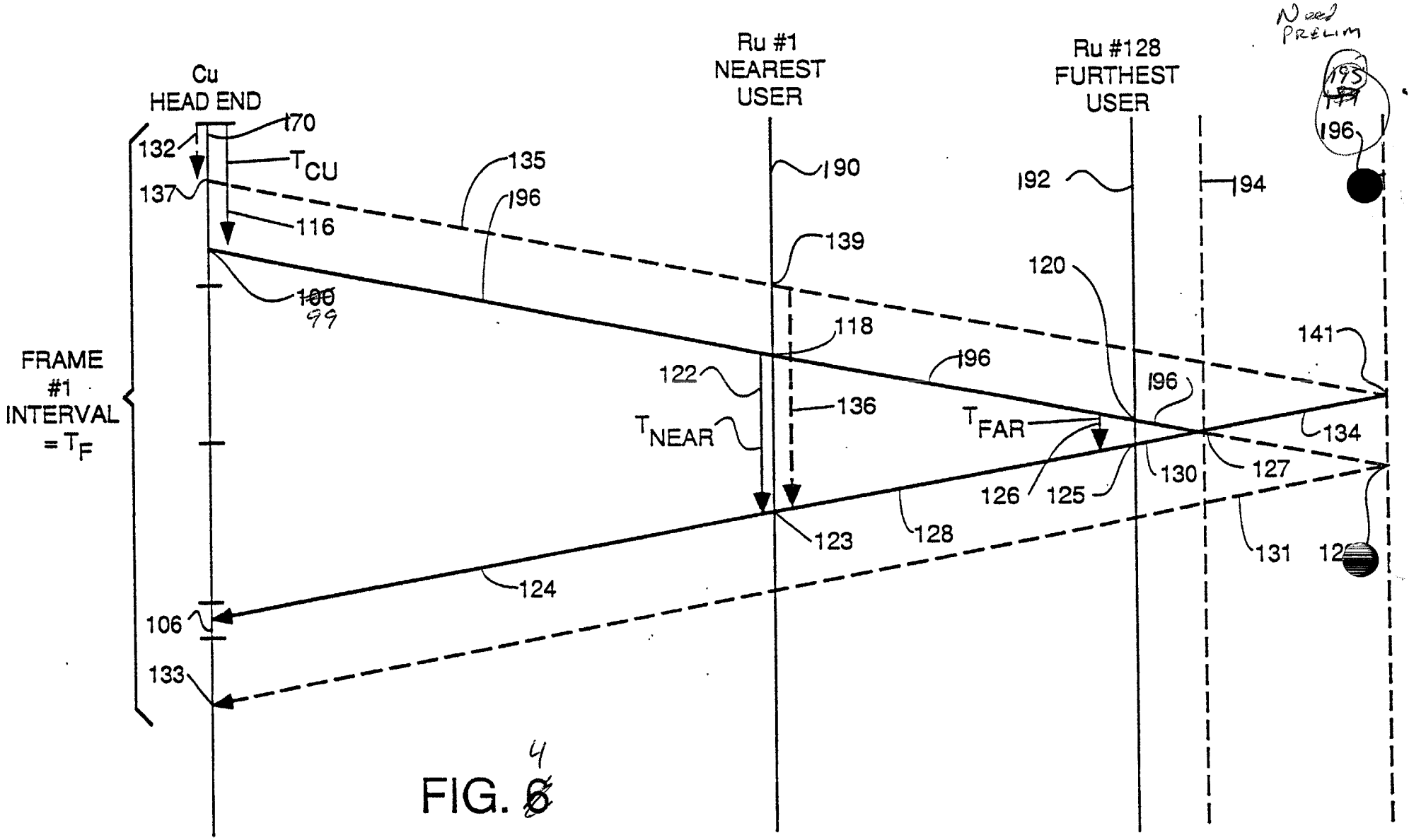
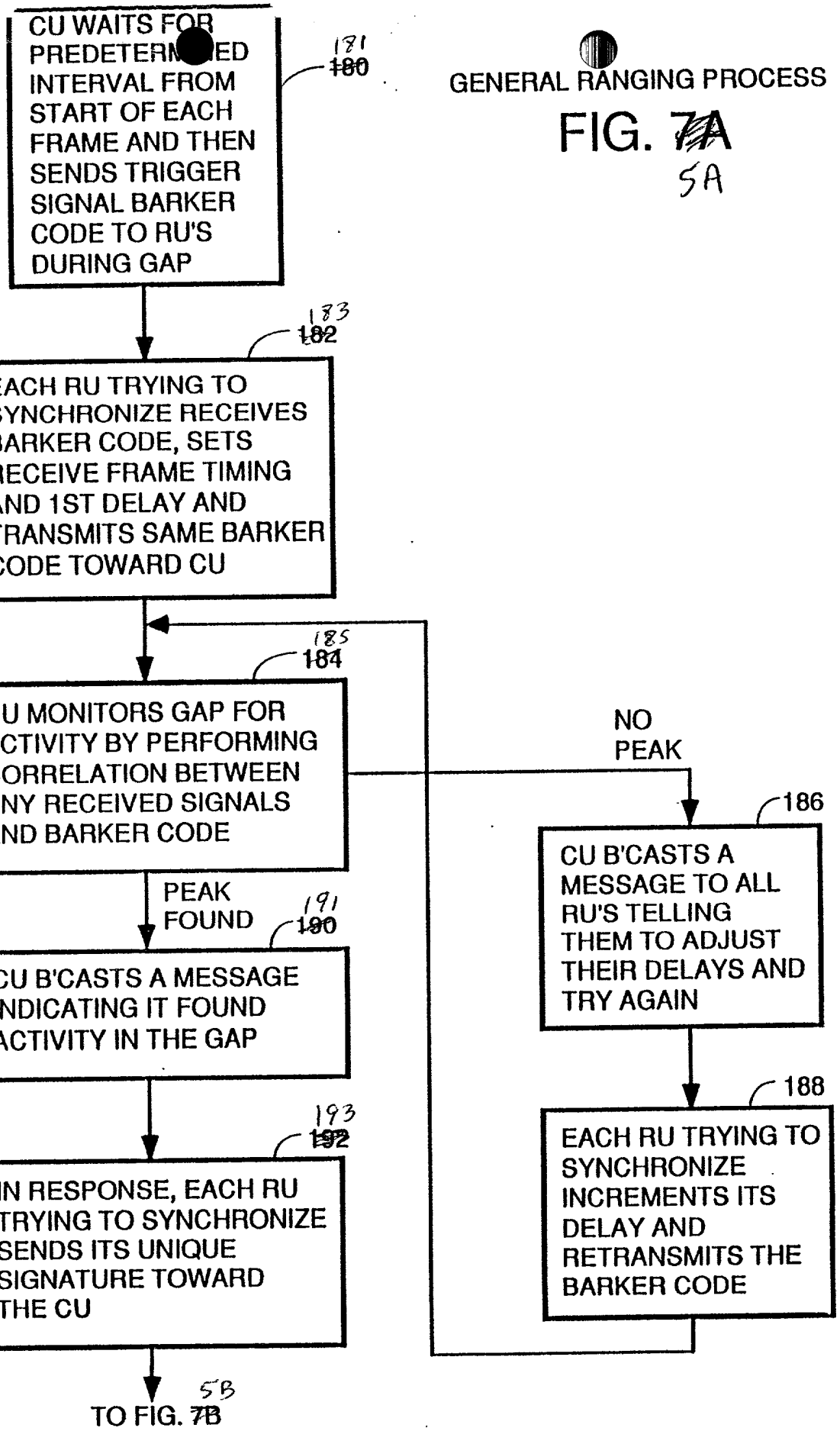

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
Need PRELIM
170
132
T_{CU}
137
116
135
196
190
139
192
194
120
196
141
118
122
196
196
136
T_{NEAR}
T_{FAR}
134
130
127
126
125
123
128
131
124
106
133
FRAME
#1
INTERVAL
$= T_F$

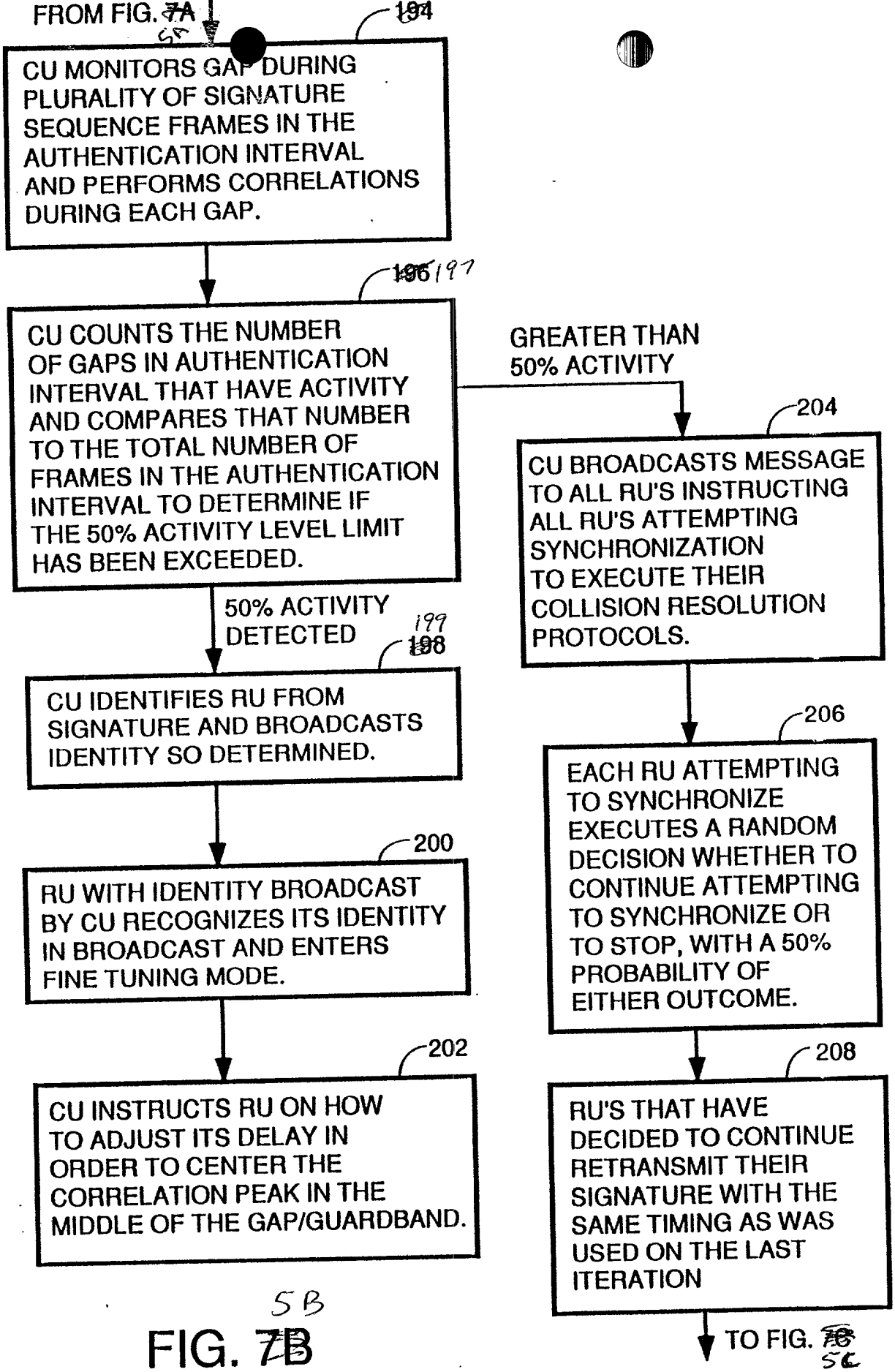
FIG. 6



GENERAL RANGING PROCESS

FIG. 7A

5A


FROM FIG. 7A
5A
194
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
196/197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
50% ACTIVITY DETECTED
199
198
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 7B
5C

5B

FIG. 7B

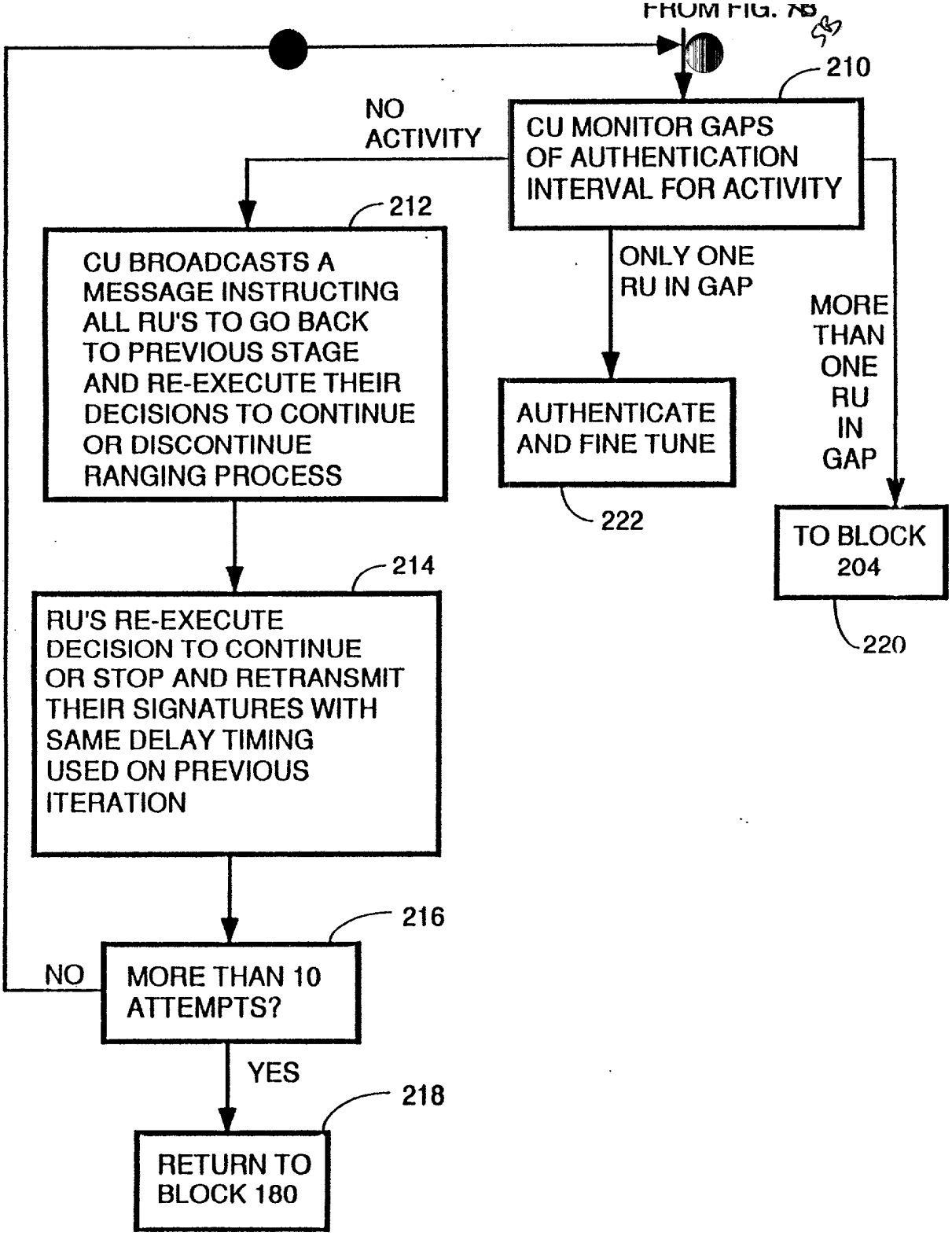
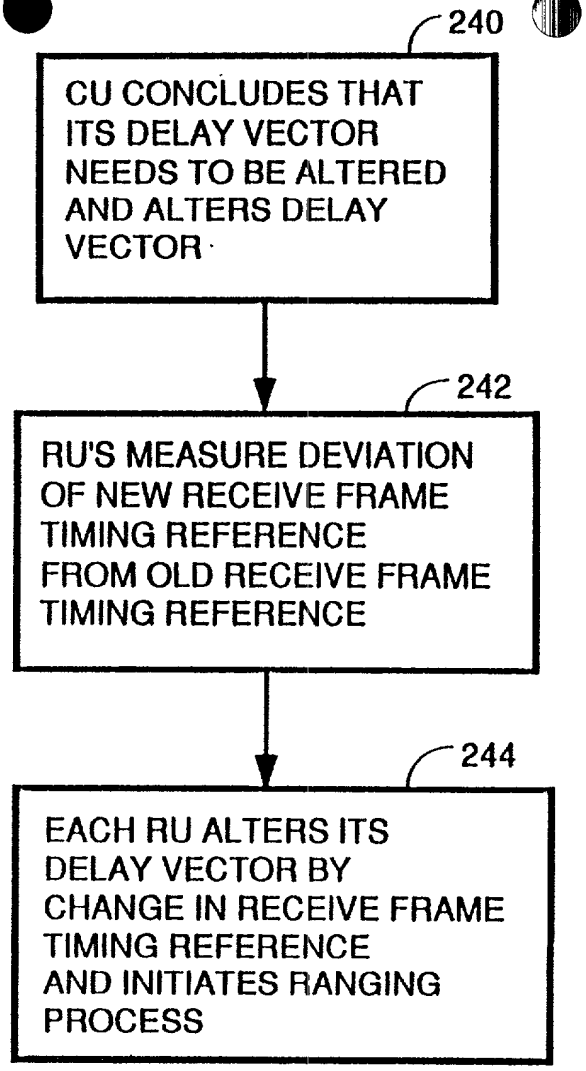

FROM FIG. 5B
210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
MORE THAN ONE RU IN GAP
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C



6

FIG. 8

DEAD RECKONING RE-SYNC

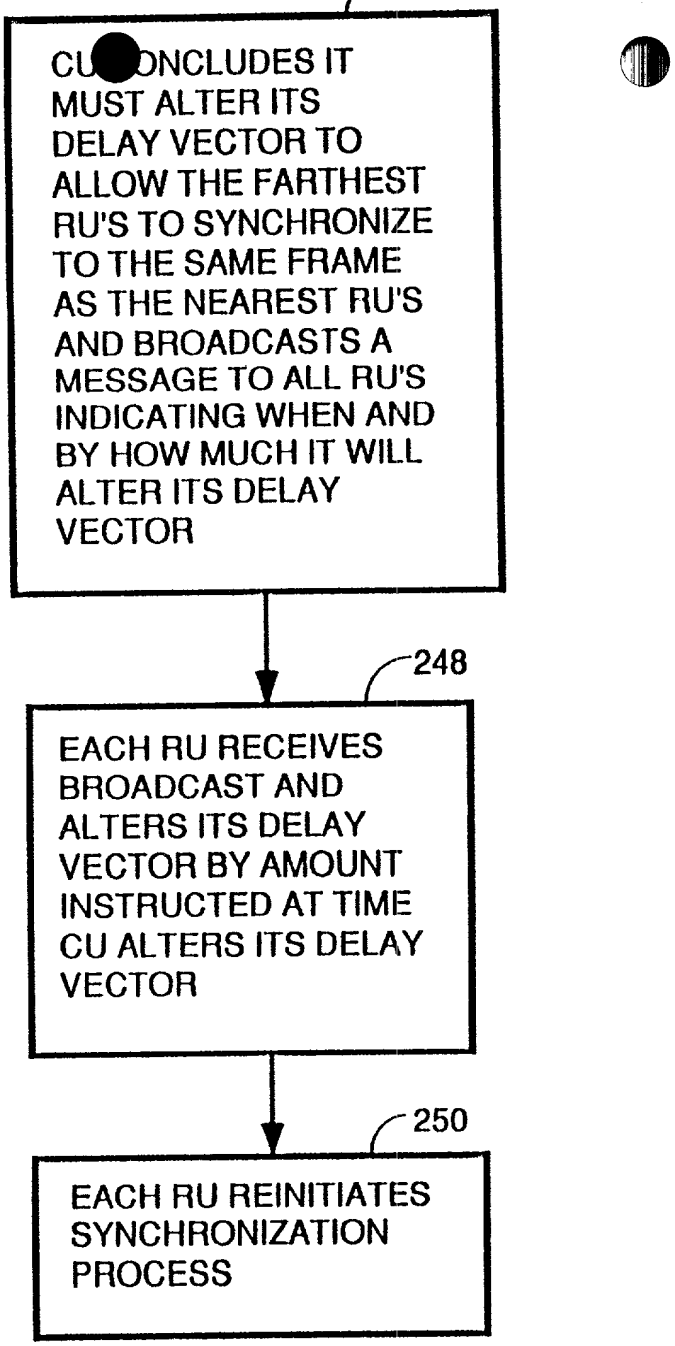
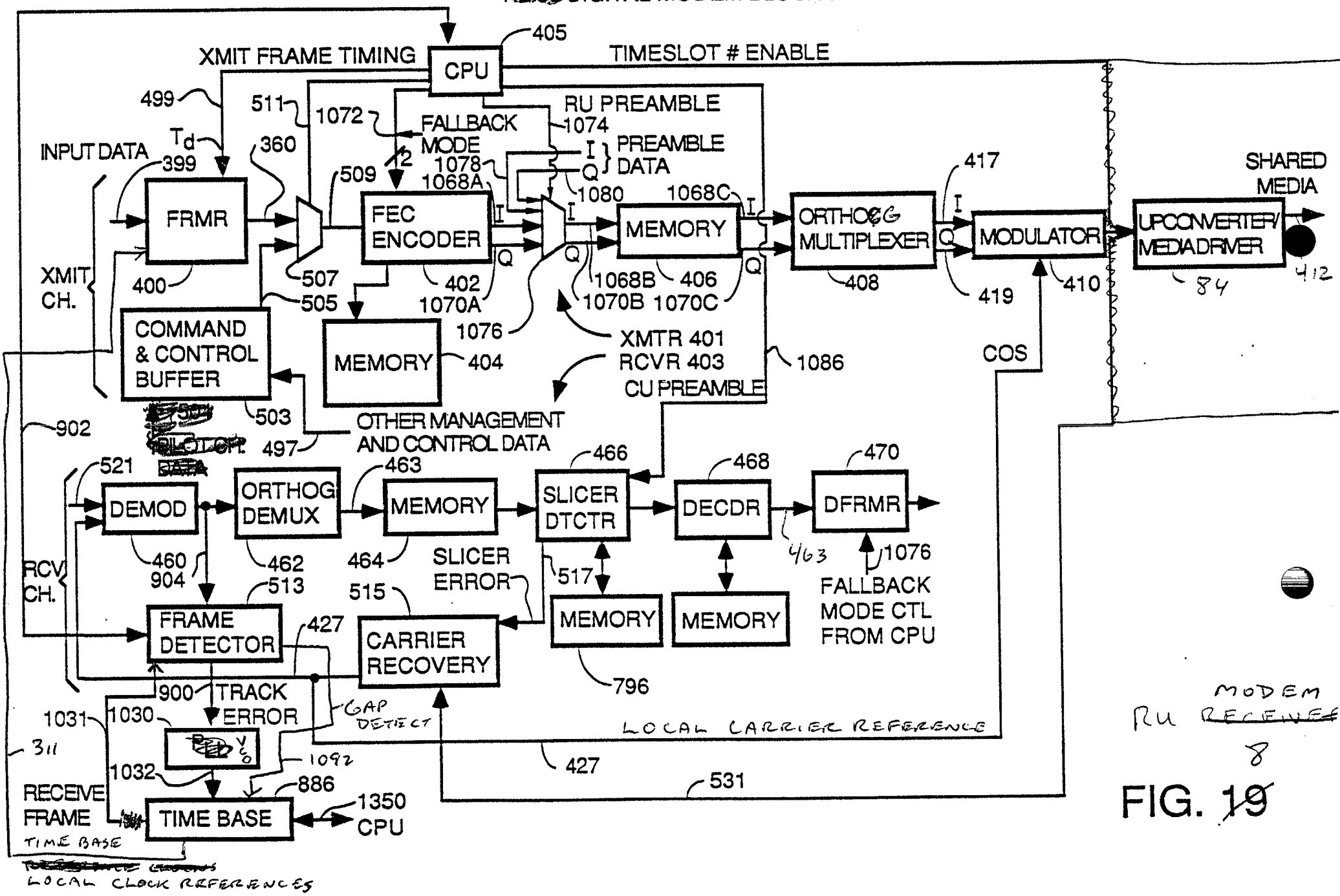


FIG. 9

PRECURSOR EMBODIMENT

DIGITAL MODEM BLOCK DIAGRAM



MODEM RU RECEIVE

8

FIG. 19

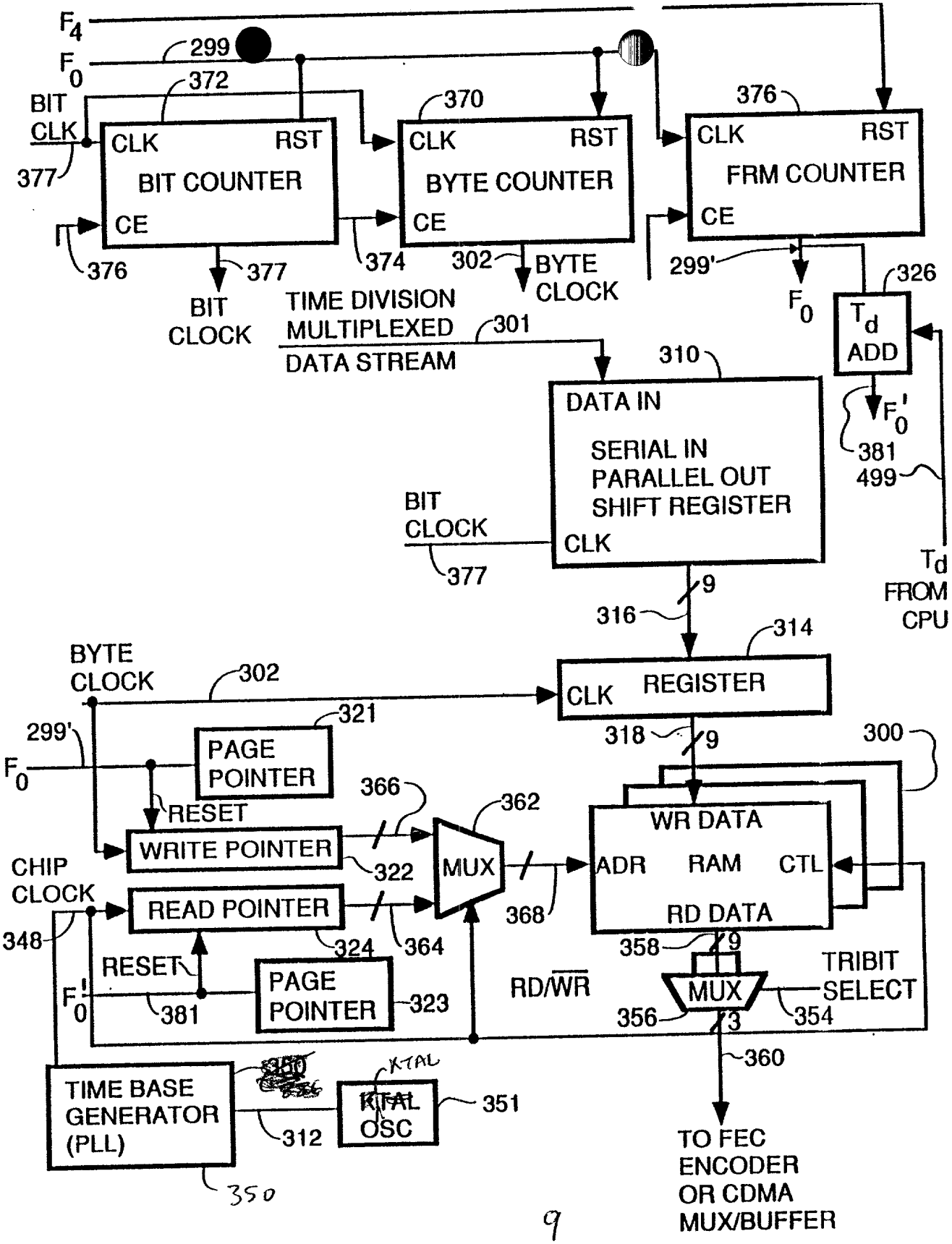

F4
F0
299
372
BIT CLK
377
CLK
RST
BIT COUNTER
CE
376
377
BIT CLOCK
374
370
CLK
RST
BYTE COUNTER
CE
302
BYTE CLOCK
376
CLK
RST
FRM COUNTER
CE
299'
F0
326
Td ADD
F'0
381
499
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
CLK
BIT CLOCK
377
Td FROM CPU
9
316
314
CLK
REGISTER
BYTE CLOCK
302
299'
F0
321
PAGE POINTER
RESET
318
9
300
366
362
WRITE POINTER
322
MUX
WR DATA
ADR
RAM
CTL
RD DATA
CHIP CLOCK
348
READ POINTER
324
364
368
358
9
RESET
F'0
381
PAGE POINTER
323
RD/WR
MUX
TRIBIT SELECT
356
3
354
360
TIME BASE GENERATOR (PLL)
312
XTAL OSC
351
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 12

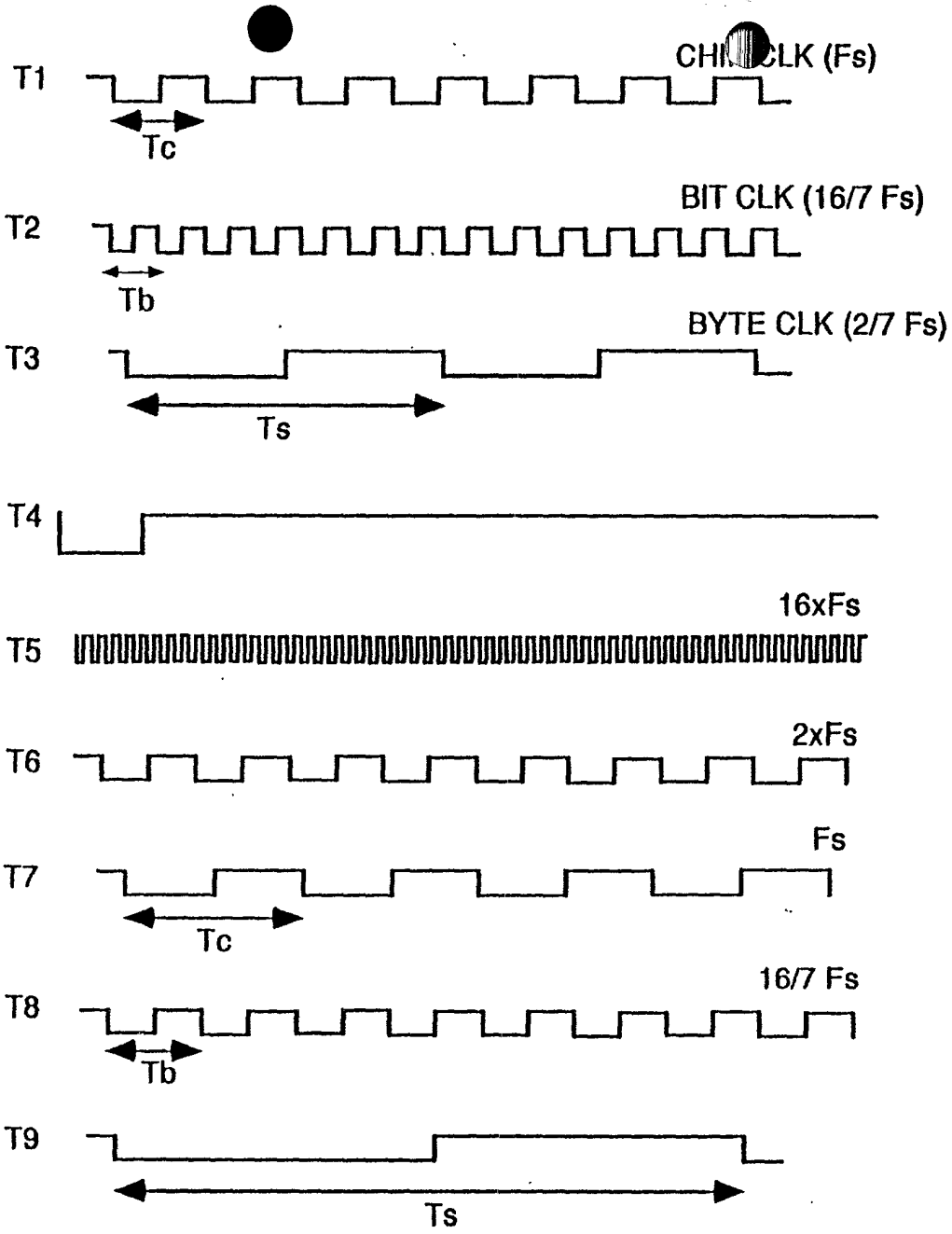
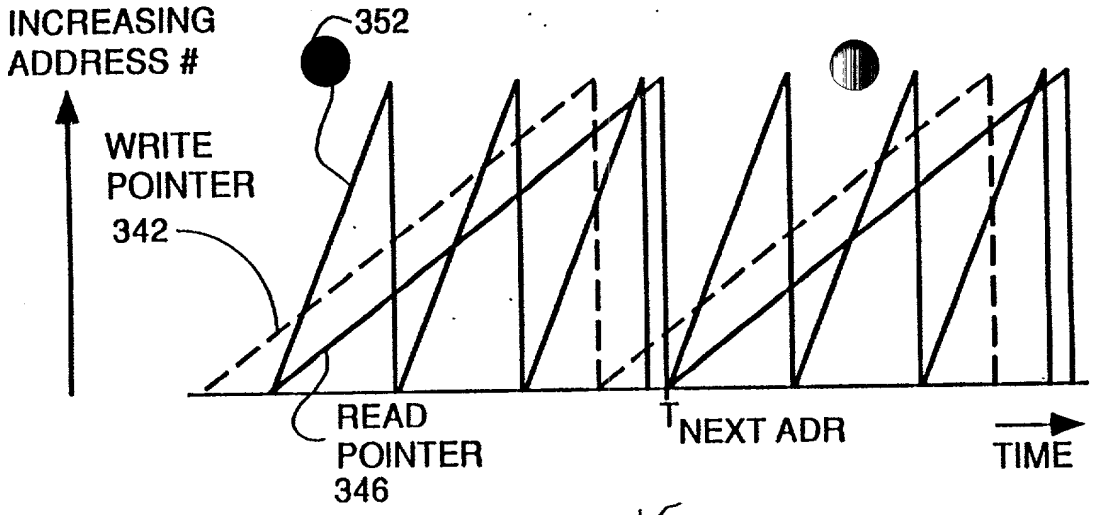
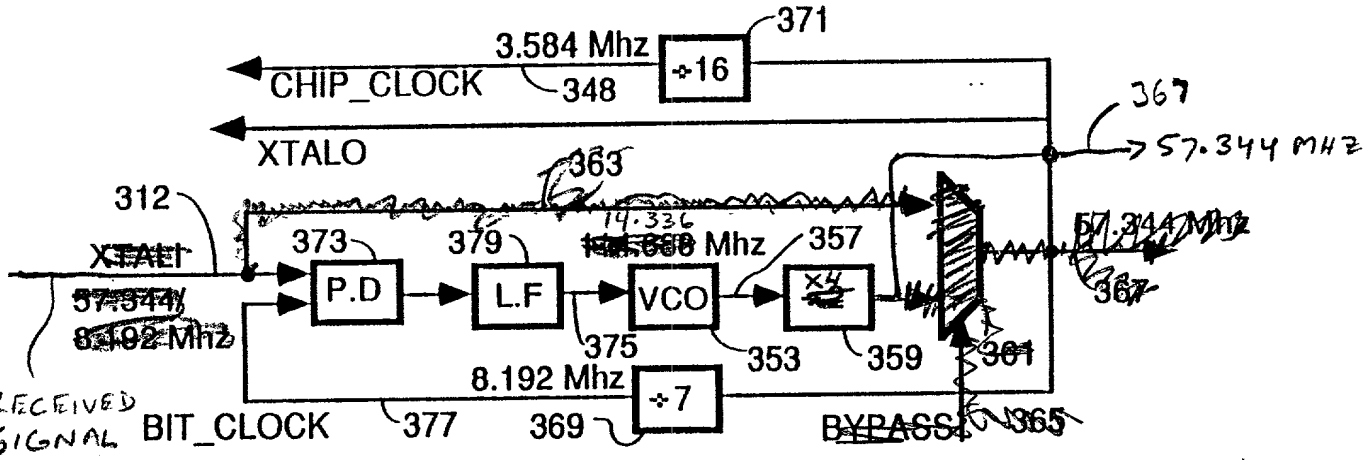

T1
CHI CLK (Fs)
Tc
T2
BIT CLK (16/7 Fs)
Tb
T3
BYTE CLK (2/7 Fs)
Ts
T4
T5
16xFs
T6
2xFs
T7
Fs
Tc
T8
16/7 Fs
Tb
T9
Ts

FIG. 10/13



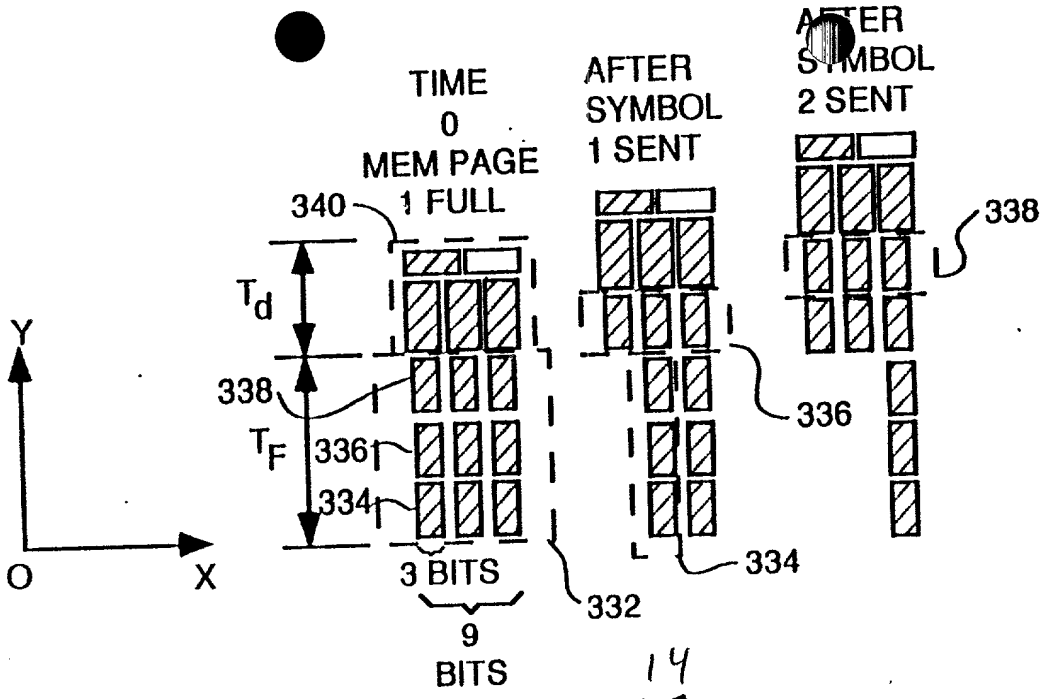
15

FIG. ~~17~~



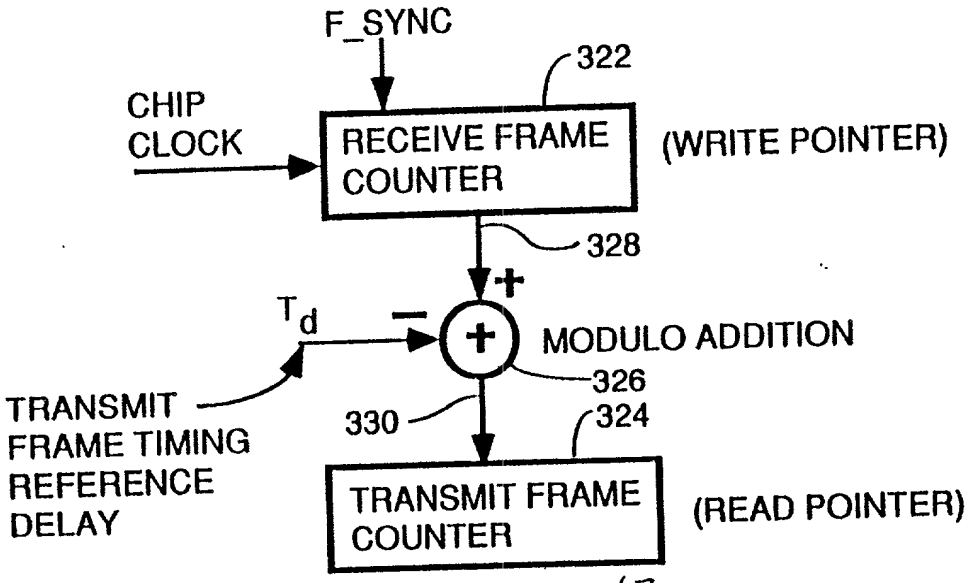
11

FIG. ~~18~~



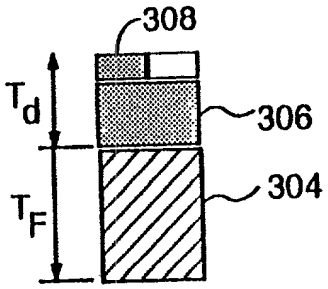
14

FIG. 14 OK



12

FIG. 15



13

FIG. 16

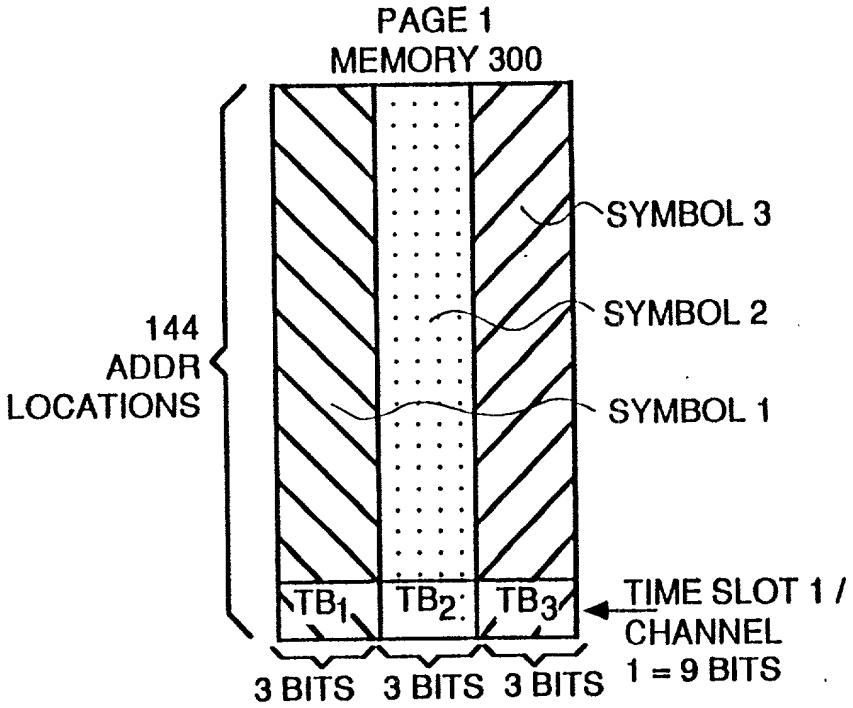
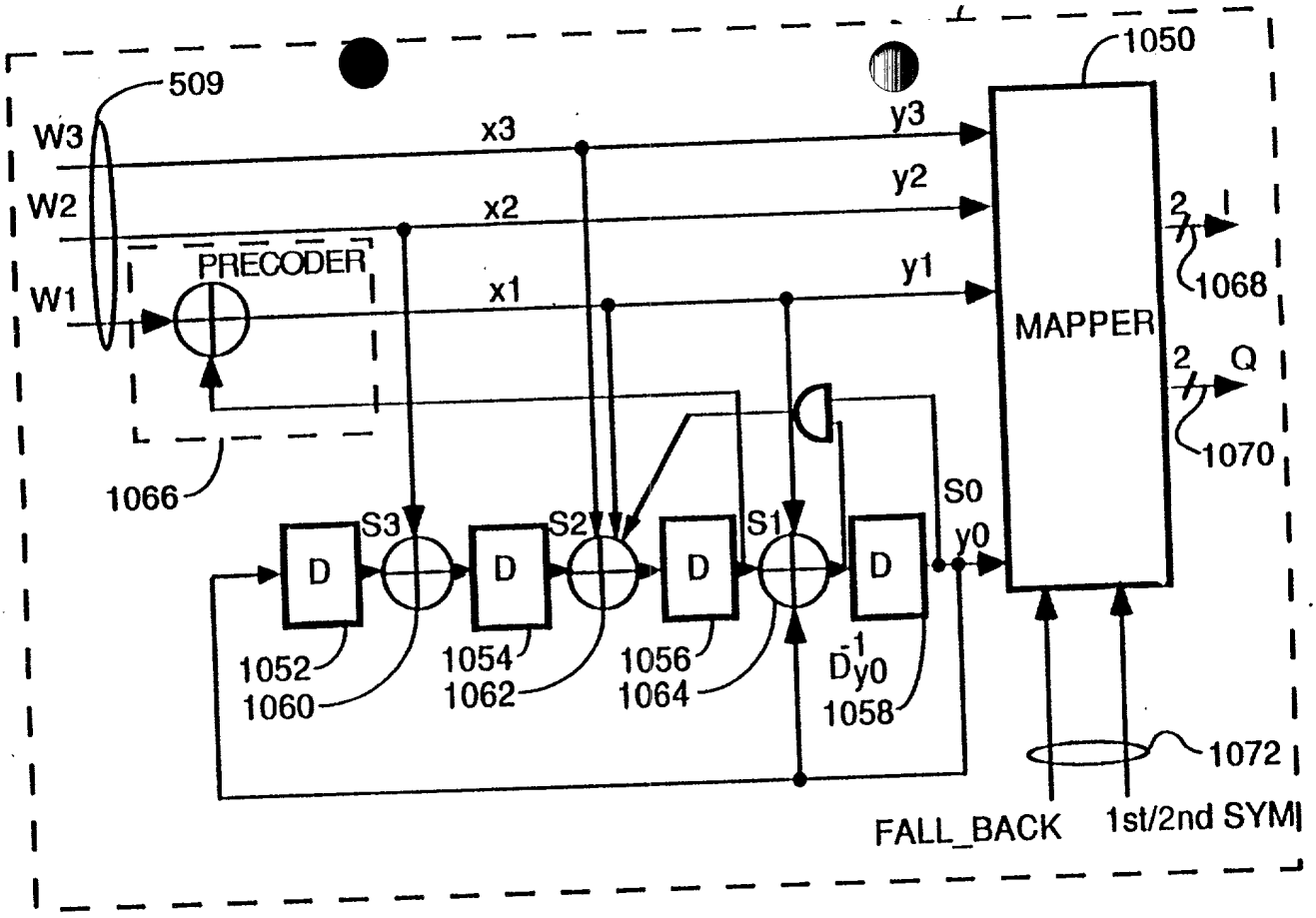

PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. 20

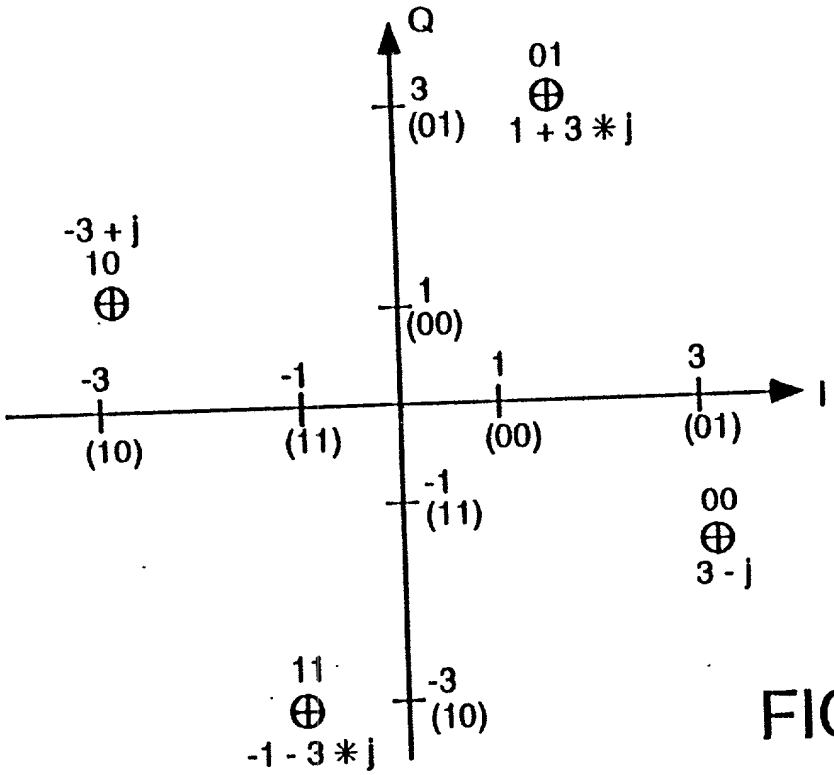


PREFERRED TRELLIS ENCODER

FIG. 42

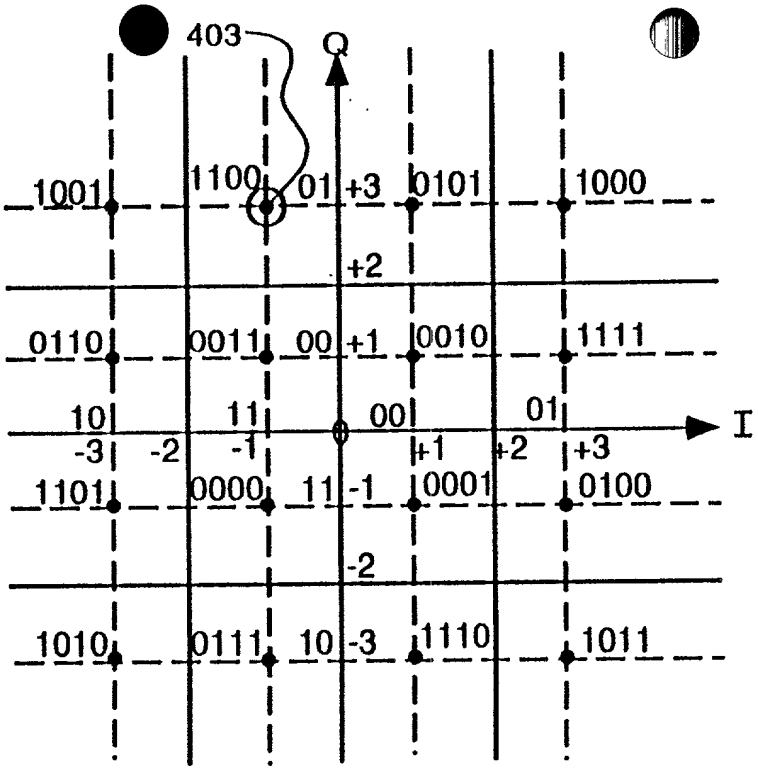
17

MAPPING FOR FALL-BACK MODE - LSB'S



21

FIG. 43



18

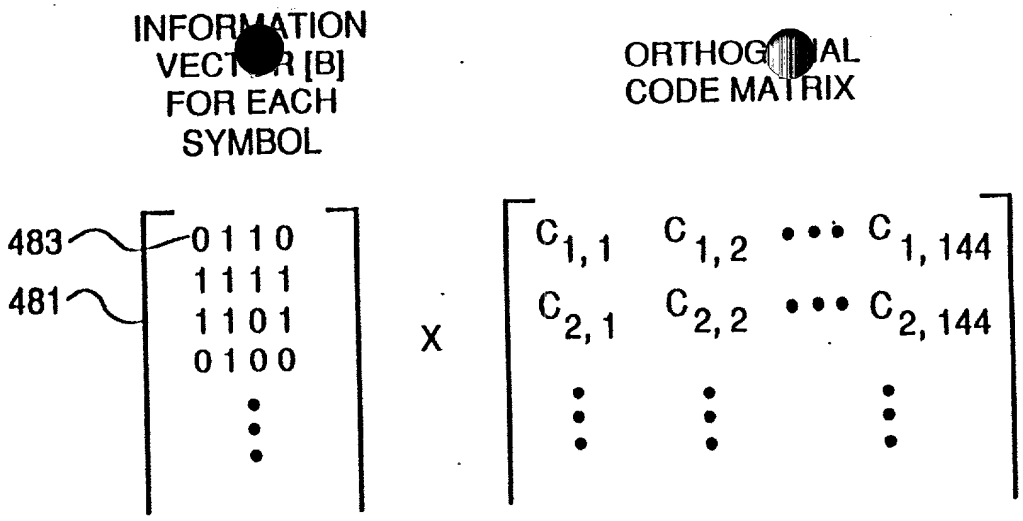
FIG. 21

CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 - j
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3* j
1001	101	011	= -3 + 3* j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
1100	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

403

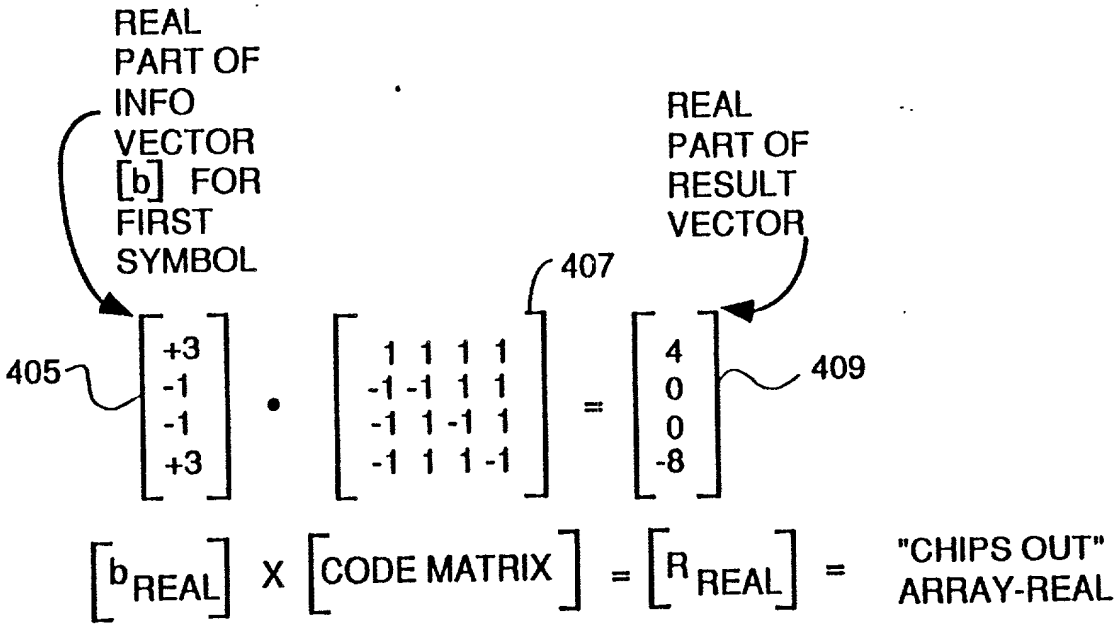
19

FIG. 22



20A

FIG. ~~23~~A



20B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

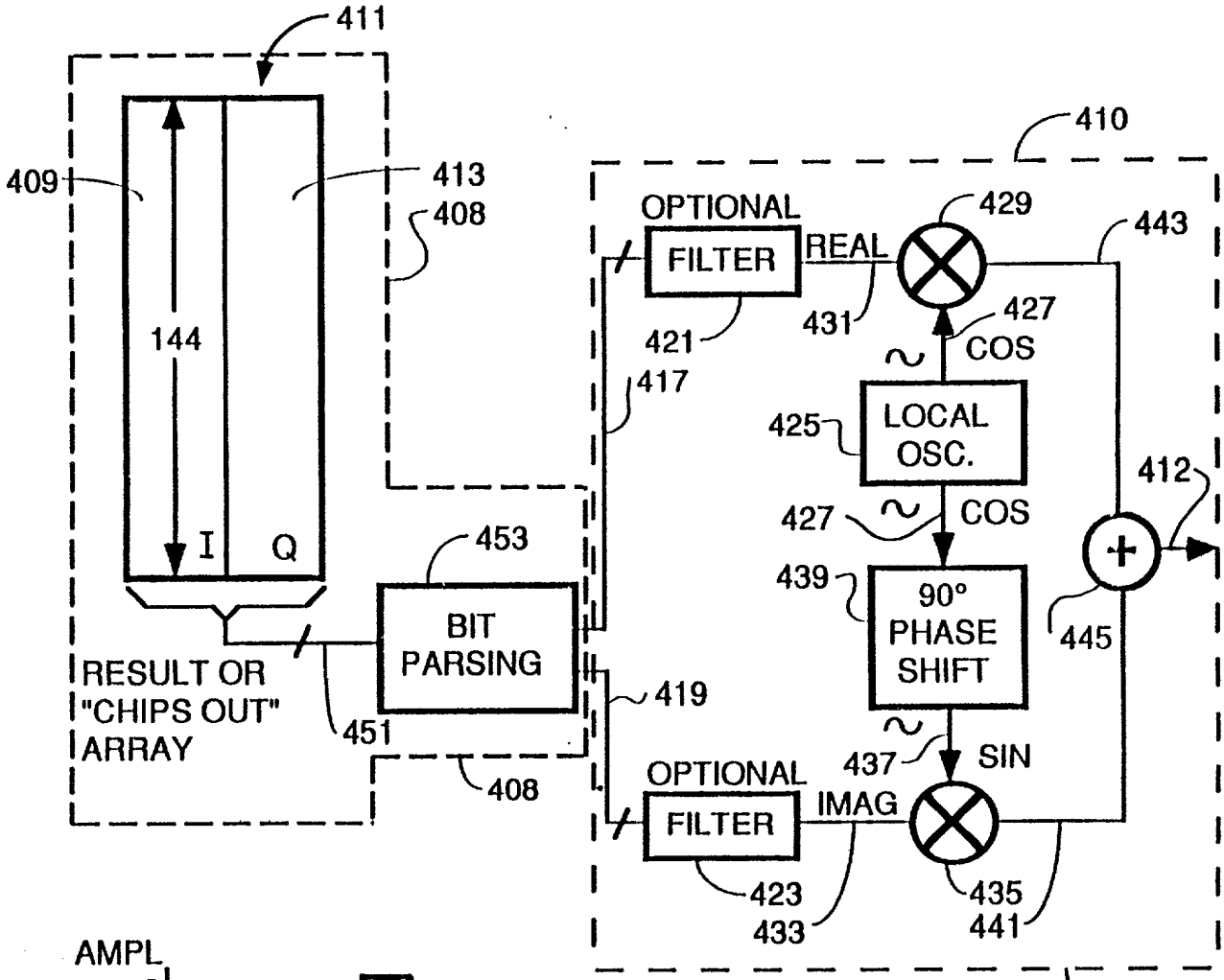

411
409
413
408
144
I
Q
RESULT OR
"CHIPS OUT"
ARRAY
451
453
BIT
PARSING
408
410
OPTIONAL
FILTER
REAL
421
431
429
443
427
COS
417
425
LOCAL
OSC.
412
427
COS
439
90°
PHASE
SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 24

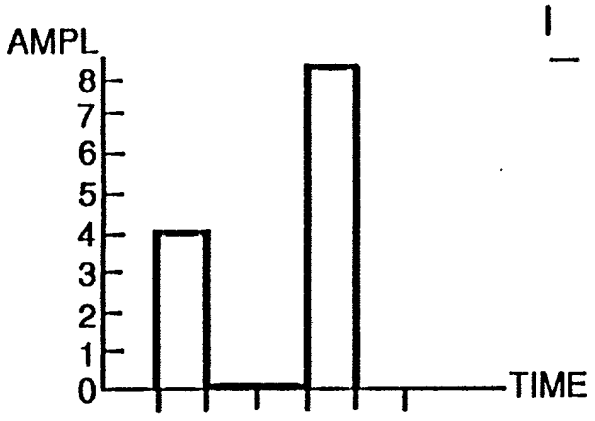
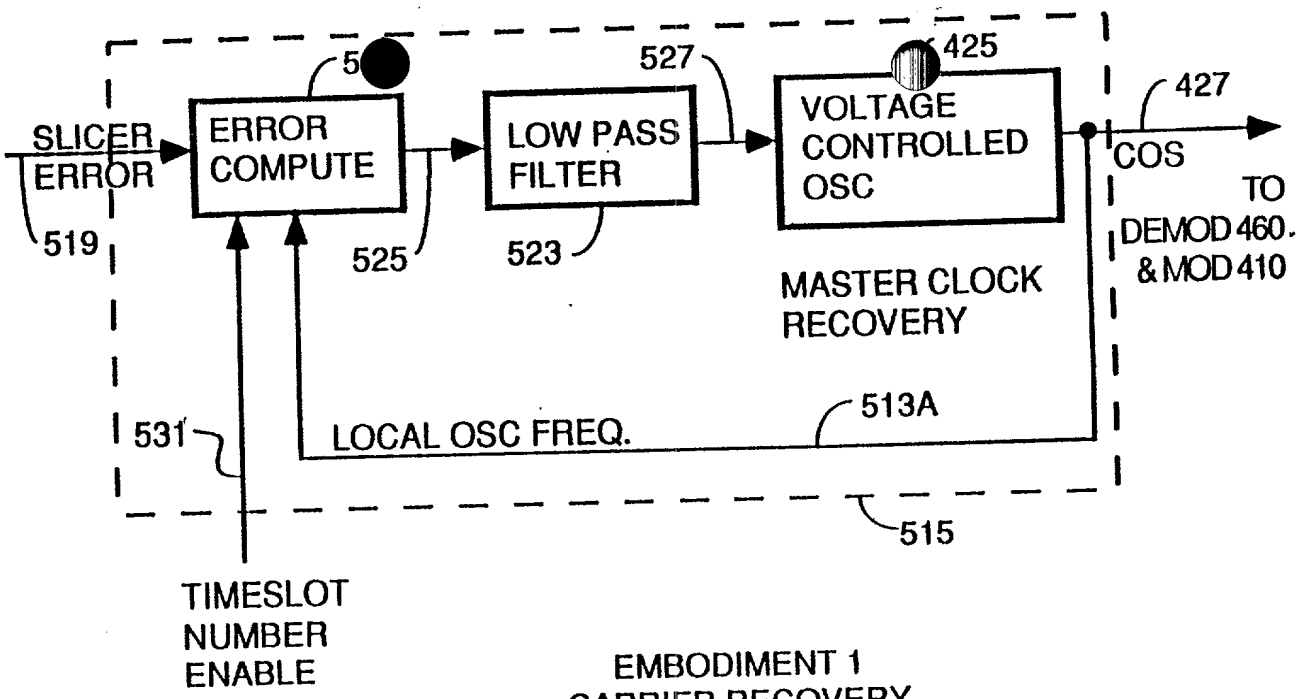

AMPL
8
7
6
5
4
3
2
1
0
TIME

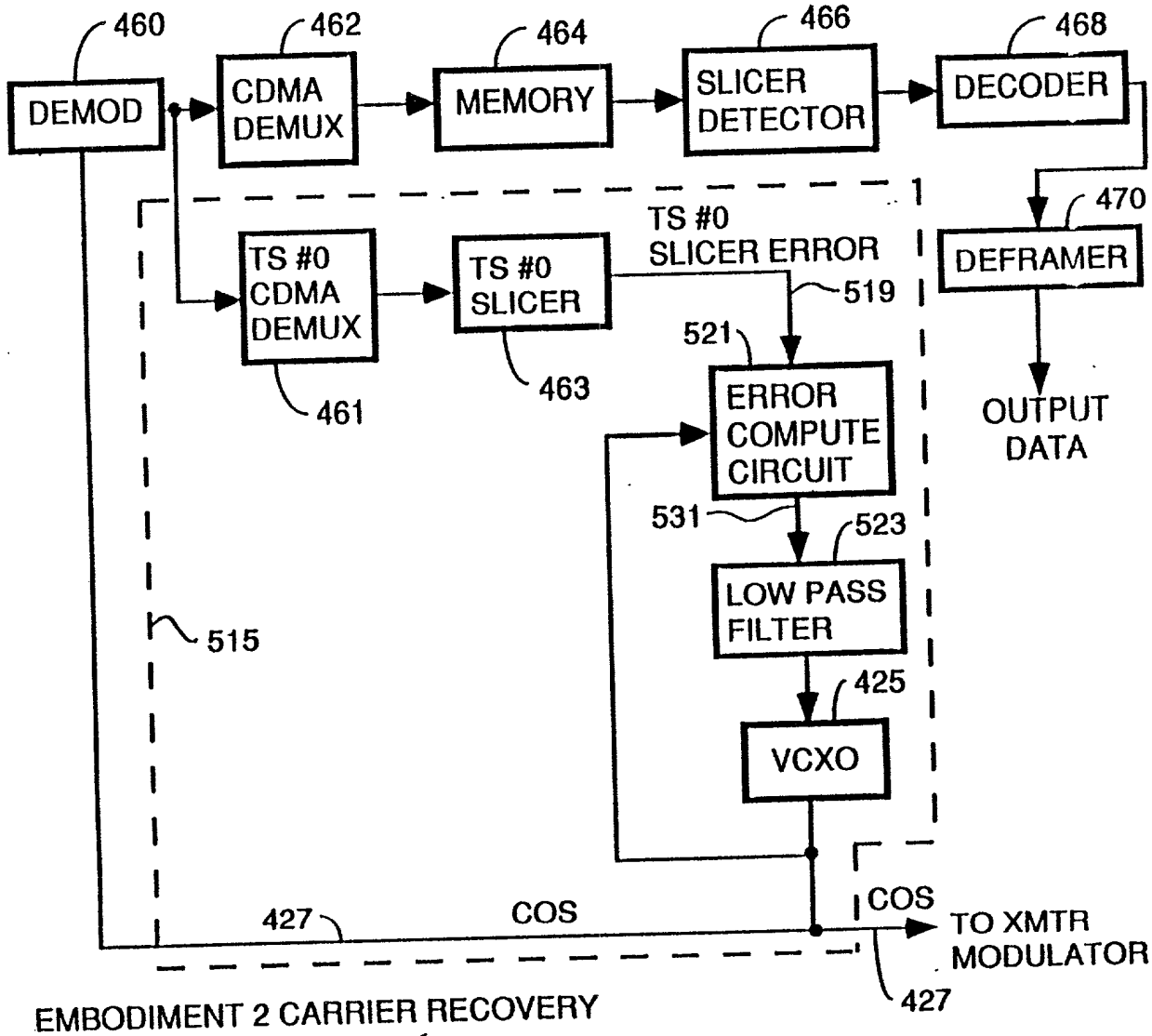
FIG. 25



EMBODIMENT 1
CARRIER RECOVERY

FIG. 35

25



EMBODIMENT 2 CARRIER RECOVERY

FIG. 36

26

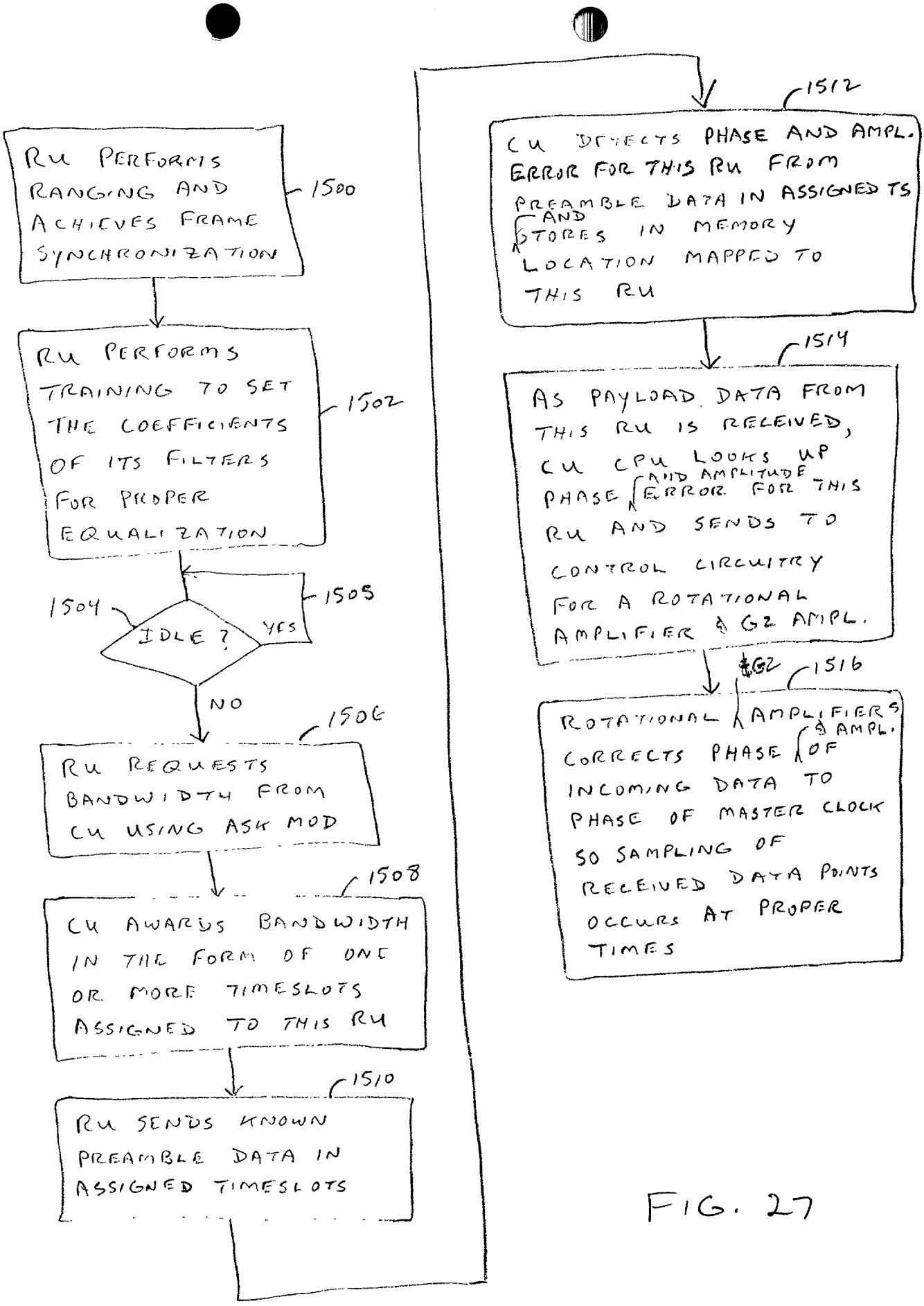

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1506
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1508
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1510
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1512
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1514
&G2
ROTATIONAL AMPLIFIERS & AMPL. CORRECTS PHASE OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES
1516

FIG. 27

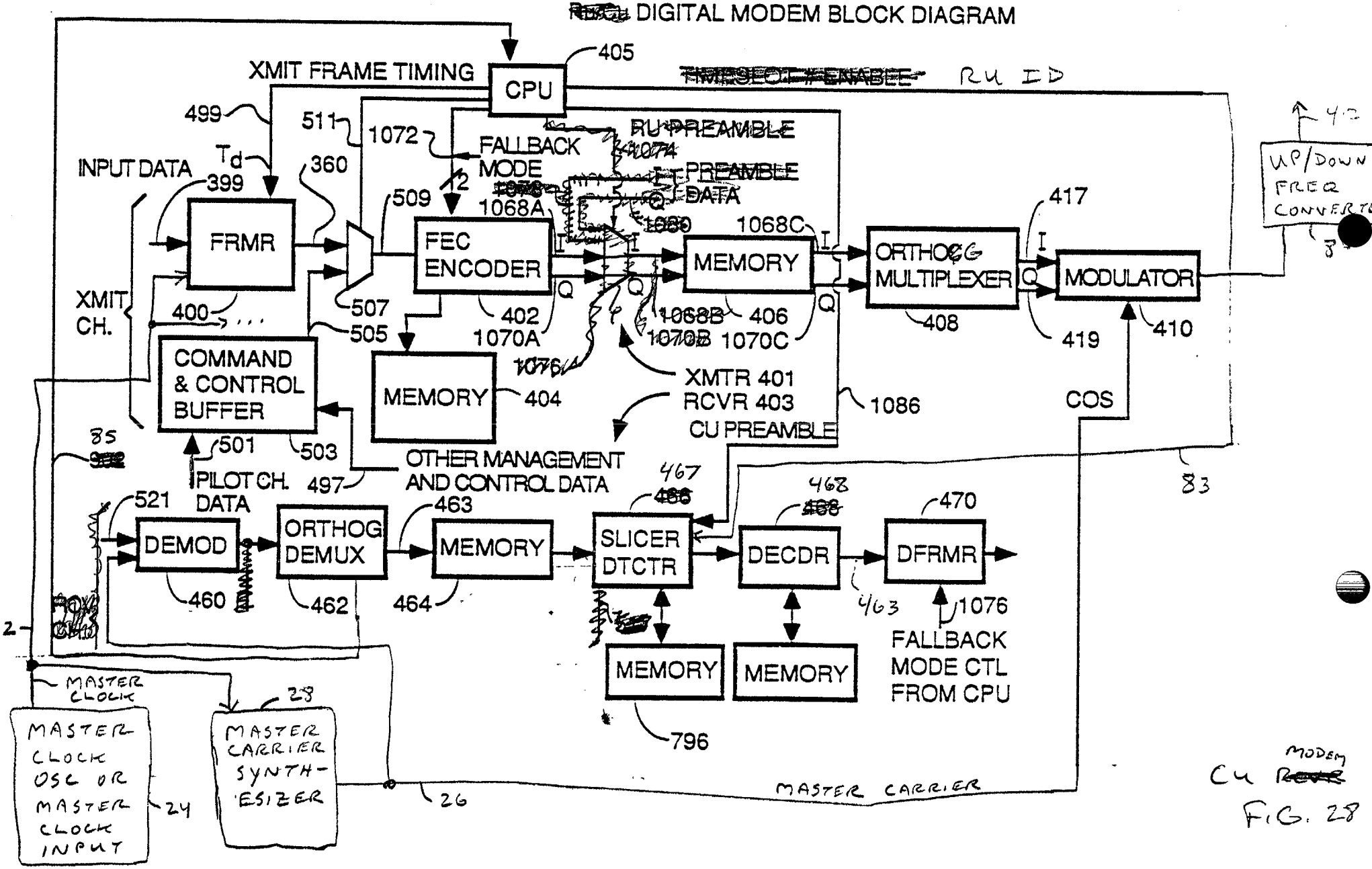

DIGITAL MODEM BLOCK DIAGRAM
XMIT FRAME TIMING
CPU
405
RU ID
499
511
1072
FALLBACK MODE
RU PREAMBLE
PREAMBLE
DATA
INPUT DATA
Td
399
360
509
2
1068A
FRMR
FEC ENCODER
MEMORY
1068C
ORTHOG MULTIPLEXER
MODULATOR
417
UP/DOWN FREQ CONVERTER
XMIT CH.
400
507
505
402
1070A
1068B
406
1070B
1070C
408
419
410
COMMAND & CONTROL BUFFER
MEMORY
404
XMTR 401
RCVR 403
CU PREAMBLE
1086
COS
85
501
503
PILOT CH. DATA
OTHER MANAGEMENT AND CONTROL DATA
497
467
468
470
521
DEMOD
ORTHOG DEMUX
463
MEMORY
SLICER DTCTR
DECDR
DFRMR
460
462
464
463
1076
FALLBACK MODE CTL FROM CPU
MEMORY
MEMORY
796
MASTER CLOCK
MASTER CLOCK OSC OR MASTER CLOCK INPUT
24
MASTER CARRIER SYNTHESIZER
26
MASTER CARRIER
MODEM
CU
83

FIG. 28

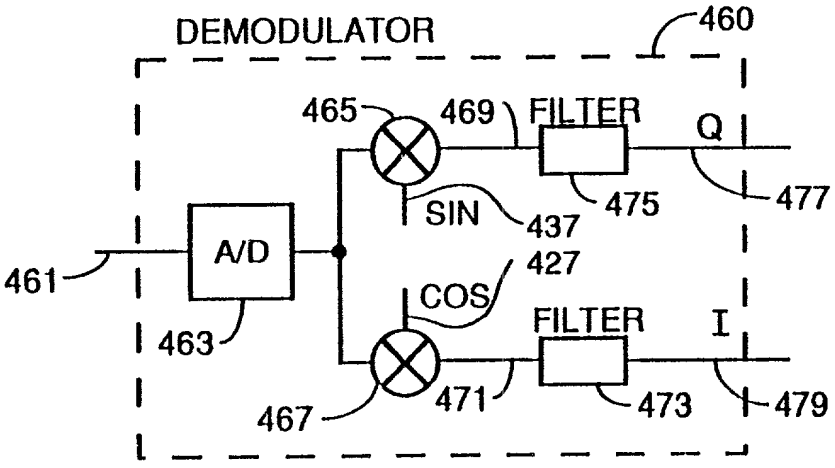

DEMODULATOR
460
465
469
FILTER
Q
475
477
SIN
437
461
A/D
427
COS
463
FILTER
I
467
471
473
479

FIG. 29

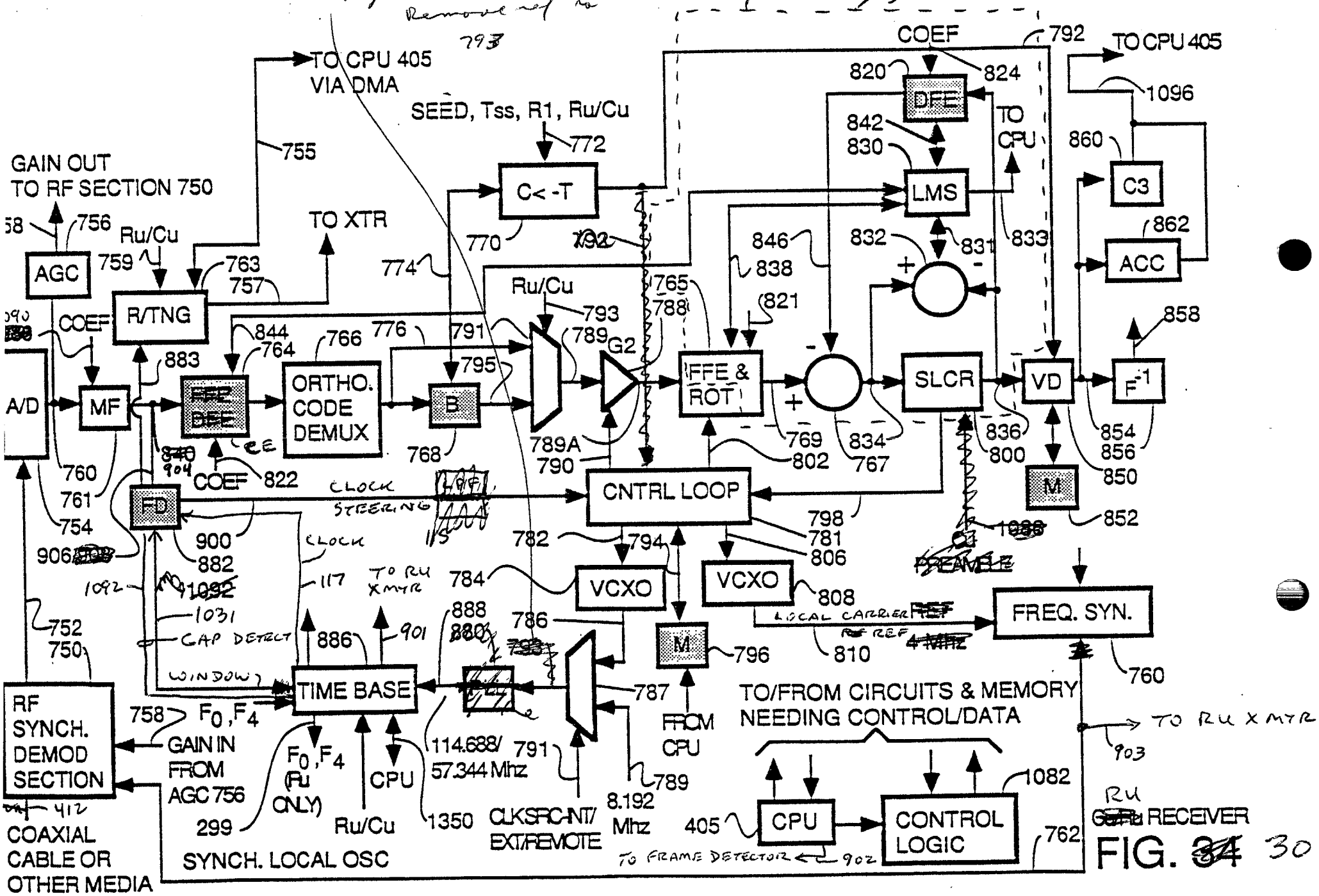

TO CPU 405 VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
GAIN OUT TO RF SECTION 750
TO XTR
COEF
792
TO CPU 405
820
824
DFE
1096
842
830
TO CPU
860
C3
LMS
862
ACC
846
838
832
831
833
Ru/Cu
759
763
757
AGC
R/TNG
774
770
C<-T
765
788
821
858
793
789
G2
776
791
795
766
764
844
883
ORTHO. CODE DEMUX
B
FFE & ROT
SLCR
VD
F-1
A/D
MF
FFE DFE
768
789A
790
769
802
834
767
836
800
854
856
850
760
761
754
906
COEF
822
CLOCK STEERING
CNTRL LOOP
FD
900
882
CLOCK
798
781
806
852
782
794
M
VCXO
VCXO
808
784
786
752
750
1092
1031
CAP DETECT
WINDOW
886
901
TO RU XMTR
117
888
880
TIME BASE
787
796
810
LOCAL CARRIER REF
FREQ. SYN.
760
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
FROM CPU
758
F0, F4
GAIN IN FROM AGC 756
RF SYNCH. DEMOD SECTION
412
COAXIAL CABLE OR OTHER MEDIA
299
F0, F4 (Ru ONLY)
CPU
Ru/Cu
1350
SYNCH. LOCAL OSC
114.688/ 57.344 Mhz
CLKSRC-INT/ EXT/REMOTE
8.192 Mhz
791
789
405
CPU
CONTROL LOGIC
1082
762
TO FRAME DETECTOR
902
TO RU XMTR
903
RU RECEIVER

FIG. 30

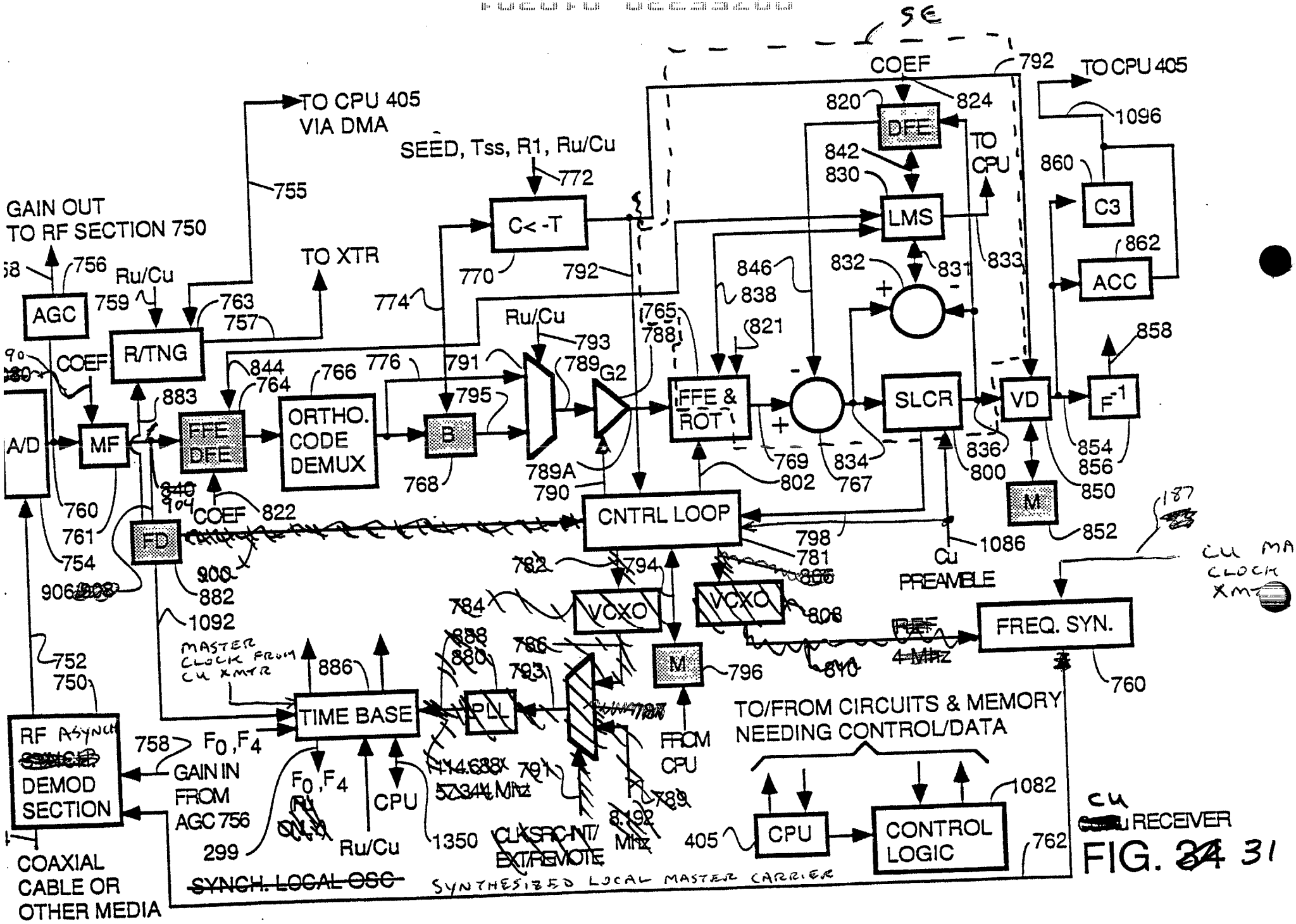

SE
COEF
792
TO CPU 405
820
824
DFE
1096
TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
772
842
830
TO CPU
860
C3
755
LMS
GAIN OUT
TO RF SECTION 750
C<-T
862
ACC
TO XTR
846
832
831
833
756
Ru/Cu
838
770
792
774
765
788
821
858
AGC
759
763
757
Ru/Cu
793
R/TNG
COEF
844
764
766
776
791
789
G2
795
883
FFE
DFE
ORTHO.
CODE
DEMUX
B
FFE &
ROT
SLCR
VD
F-1
A/D
MF
768
789A
790
769
834
767
836
800
802
854
856
850
760
761
754
840
904
COEF
822
CNTRL LOOP
FD
M
852
187
798
781
1086
Cu
PREAMBLE
900
882
1092
782
794
784
VCXO
VCXO
808
FREQ. SYN.
MASTER
CLOCK FROM
CU XMTR
888
880
786
793
752
750
886
TIME BASE
PLL
M
796
4 MHz
760
TO/FROM CIRCUITS & MEMORY
NEEDING CONTROL/DATA
RF ASYNCH
DEMOD
SECTION
758
F0, F4
GAIN IN
FROM
AGC 756
FROM
CPU
F0, F4
CPU
Ru/Cu
1350
CLKSPCNT/
EXT/REMOTE
405
CPU
CONTROL
LOGIC
1082
762
CU
RECEIVER
COAXIAL
CABLE OR
OTHER MEDIA
299
SYNCH. LOCAL OSC
SYNTHESIZED LOCAL MASTER CARRIER

FIG. 24 31

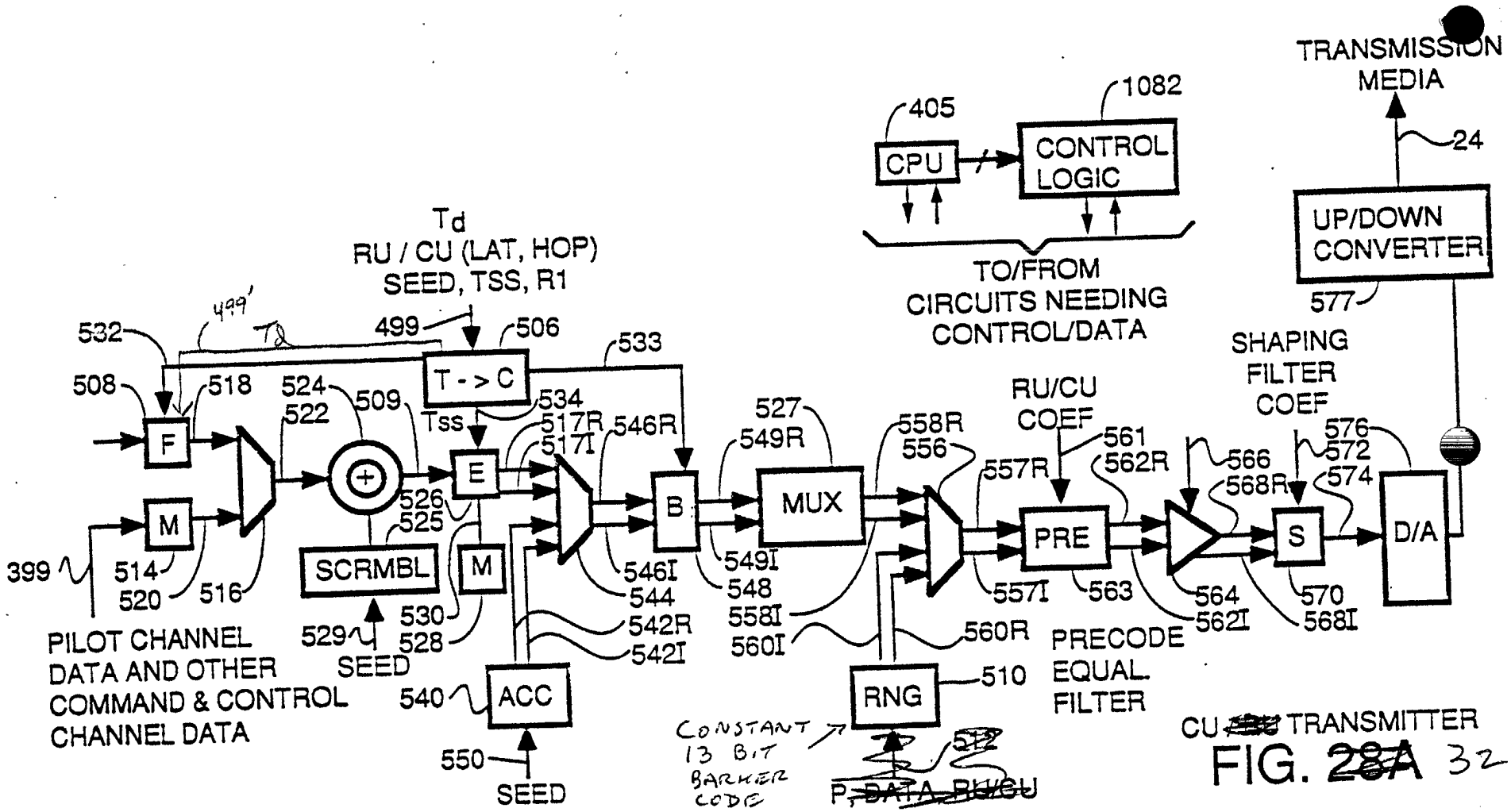

TRANSMISSION MEDIA
24
UP/DOWN CONVERTER
577
1082
405
CPU
CONTROL LOGIC
TO/FROM CIRCUITS NEEDING CONTROL/DATA
Td
RU / CU (LAT, HOP)
SEED, TSS, R1
499'
Td
499
506
533
532
508
518
524
522
509
T -> C
534
Tss
517R
517I
546R
527
549R
558R
556
RU/CU COEF
561
562R
557R
566
568R
576
572
574
SHAPING FILTER COEF
F
M
E
B
MUX
PRE
S
D/A
526
525
399
514
520
516
SCRMBL
M
546I
544
549I
548
558I
560I
557I
563
564
562I
570
568I
530
528
529
SEED
542R
542I
560R
PILOT CHANNEL DATA AND OTHER COMMAND & CONTROL CHANNEL DATA
PRECODE EQUAL FILTER
540
ACC
RNG
510
CONSTANT 13 BIT BARKER CODE
512
P-DATA-RU/CU
550
SEED
CU TRANSMITTER

FIG. 28A 32

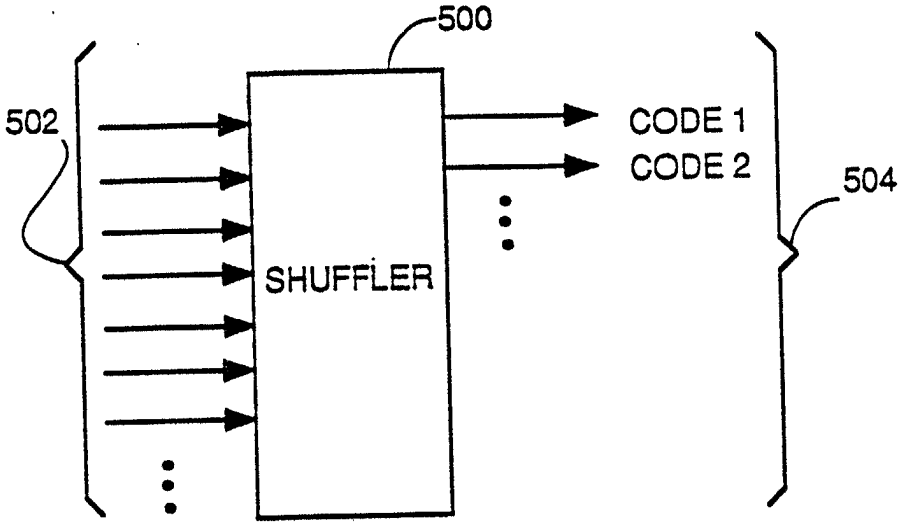


FIG. 27 38

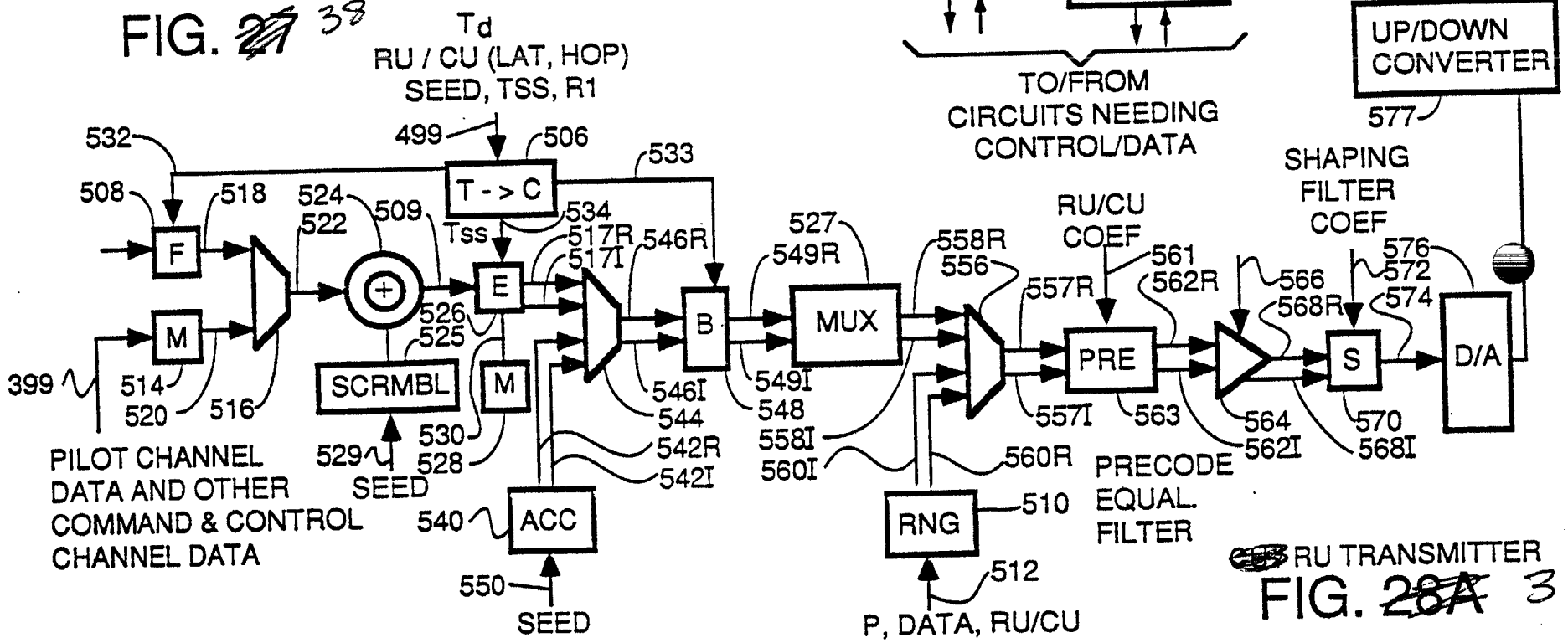
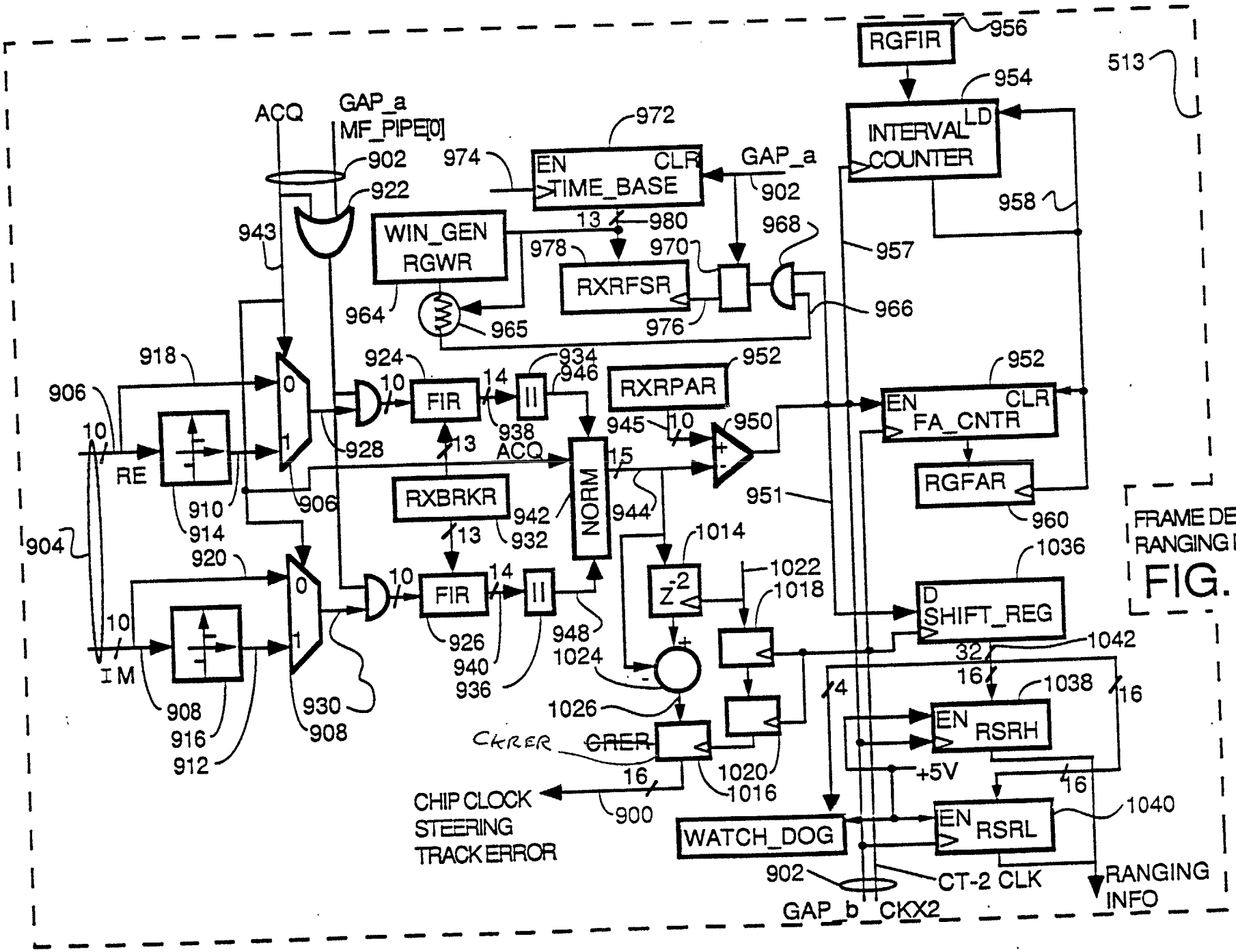


FIG. 28A 3


RGFIR
956
513
954
INTERVAL LD
COUNTER
958
957
ACQ
GAP_a
MF_PIPE[0]
902
922
943
974
EN CLR
TIME_BASE
972
GAP_a
902
968
WIN_GEN
RGWR
13
980
978
970
RXRFSR
964
965
976
966
918
906
924
10
FIR
14
934
946
938
RXRPAR
952
952
EN CLR
FA_CNTR
945
10
950
10
RE
928
13
ACQ
15
RGFAR
960
910
914
906
RXBRKR
942
932
NORM
944
951
904
920
1014
1036
FRAME DETECTOR/
RANGING DETECTOR
FIG. 38
10
FIR
14
1022
1018
D
SHIFT_REG
926
940
936
948
1024
1042
32
16
1038
16
IM
908
916
912
930
908
1026
4
EN RSRH
CKRER
CRER
1020
1016
+5V
16
16
CHIP CLOCK
STEERING
TRACK ERROR
900
WATCH_DOG
EN RSRL
1040
902
CT-2 CLK
RANGING
INFO
GAP_b CKX2

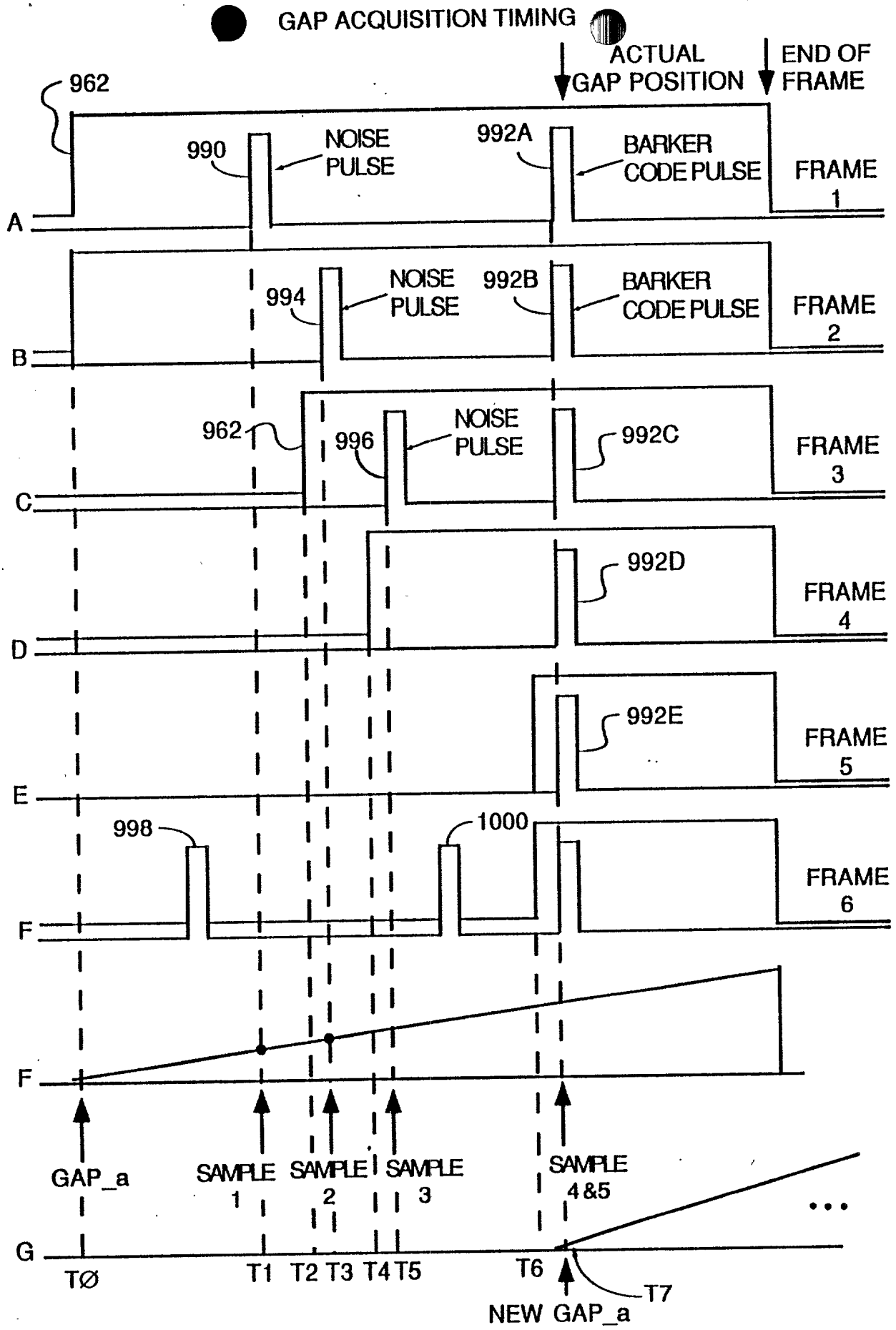
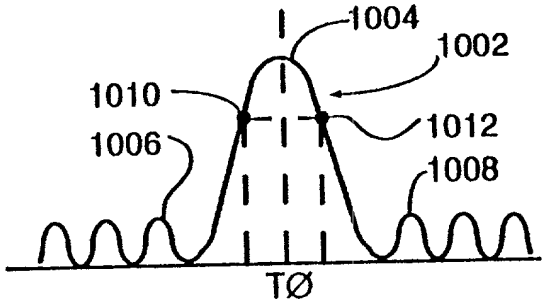
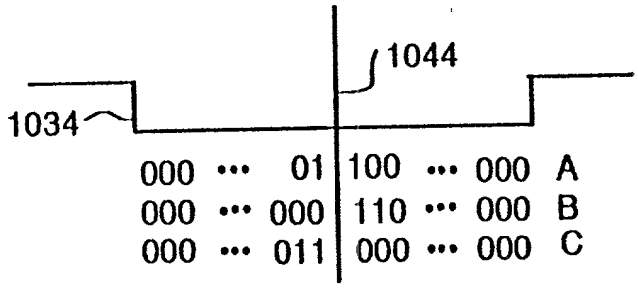

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 39 35



36

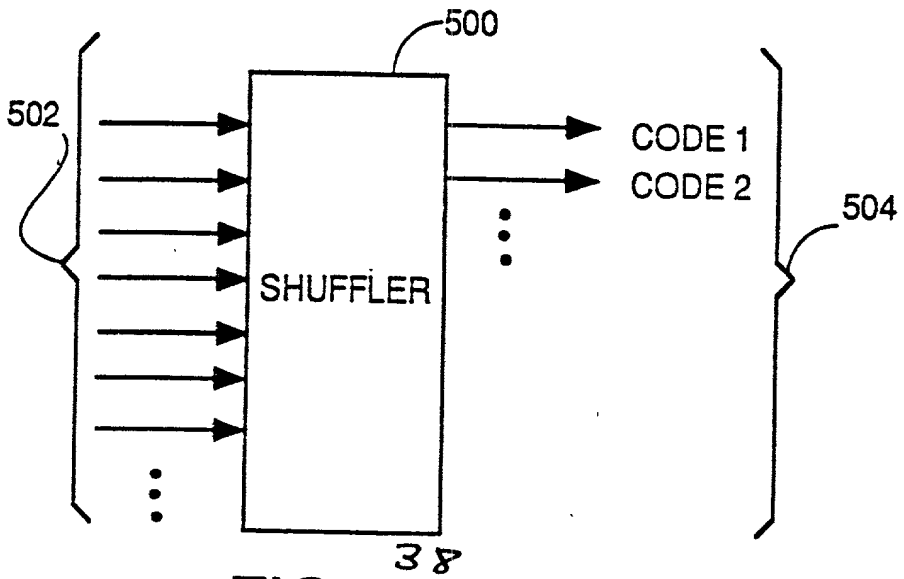
FIG. 40



37

FIG. 41

FINE TUNING TO CENTER BARKER CODE



38

FIG. 27

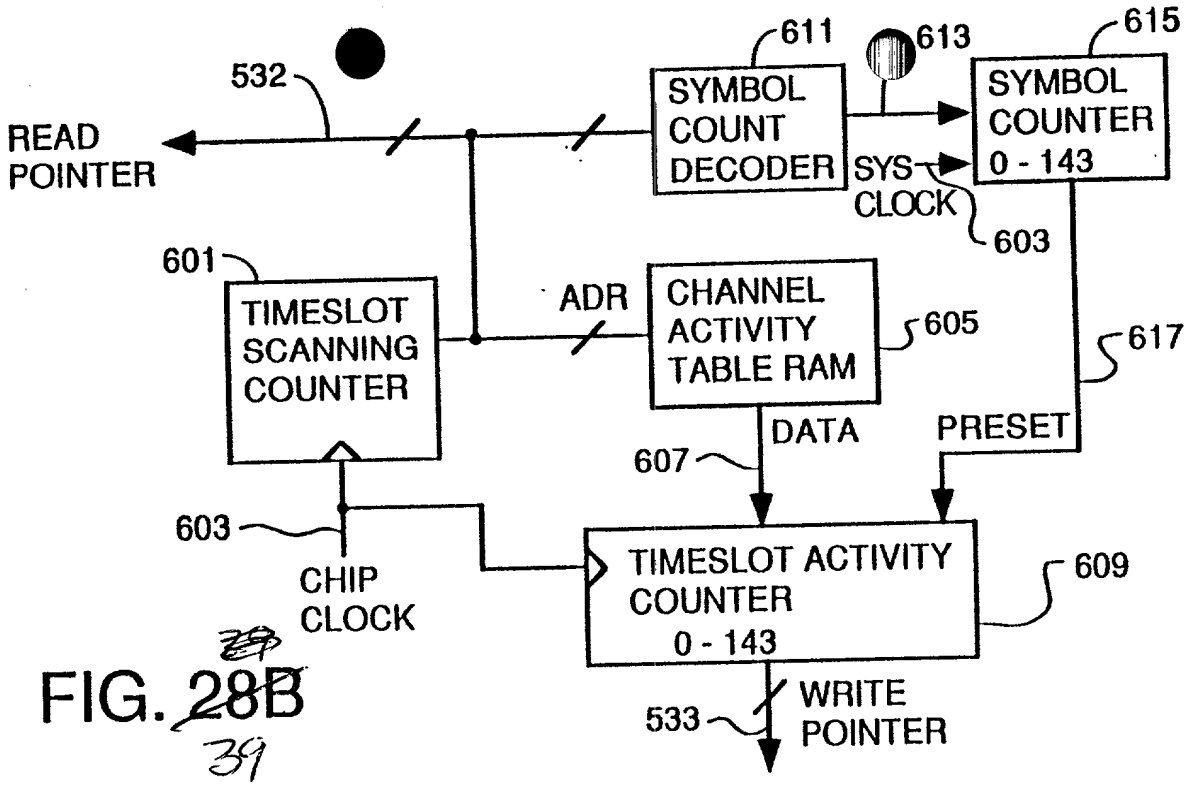


FIG. 28B

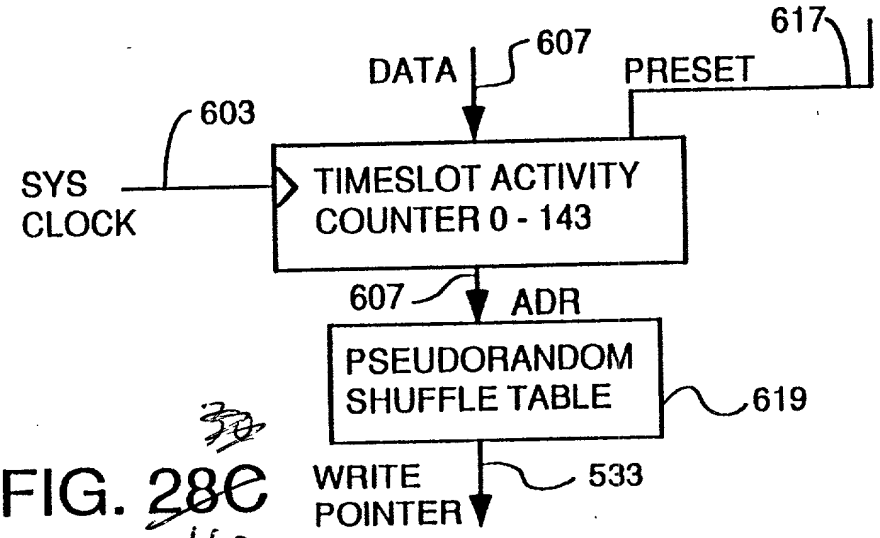


FIG. 28C

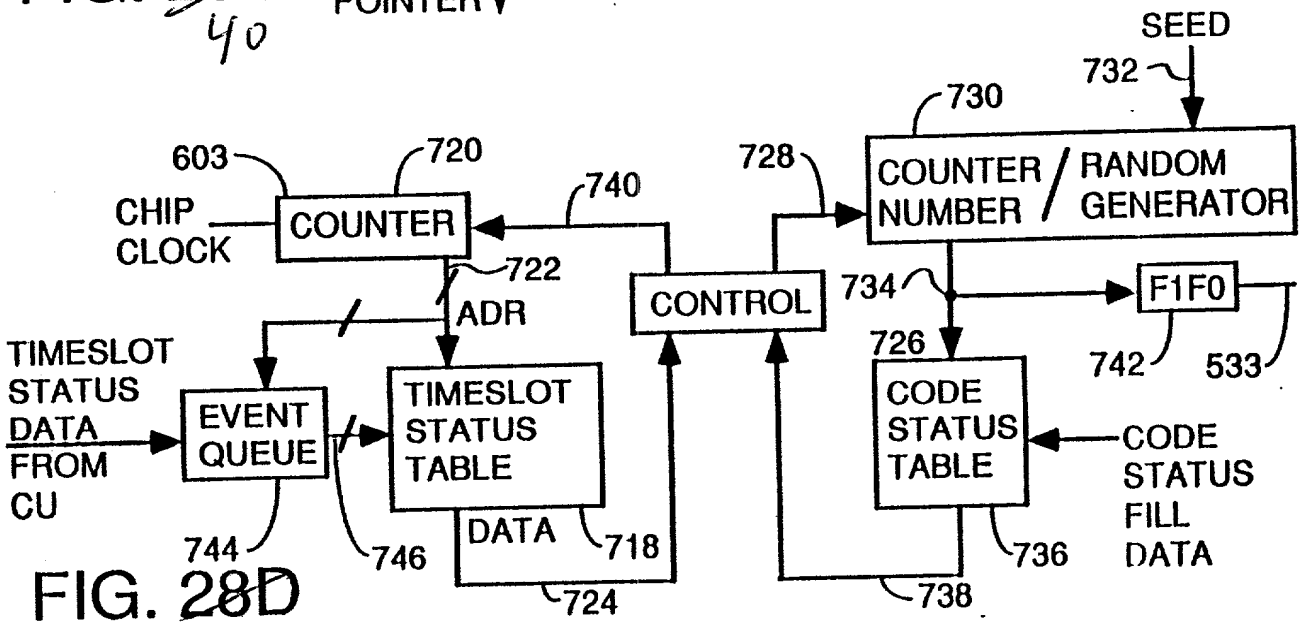
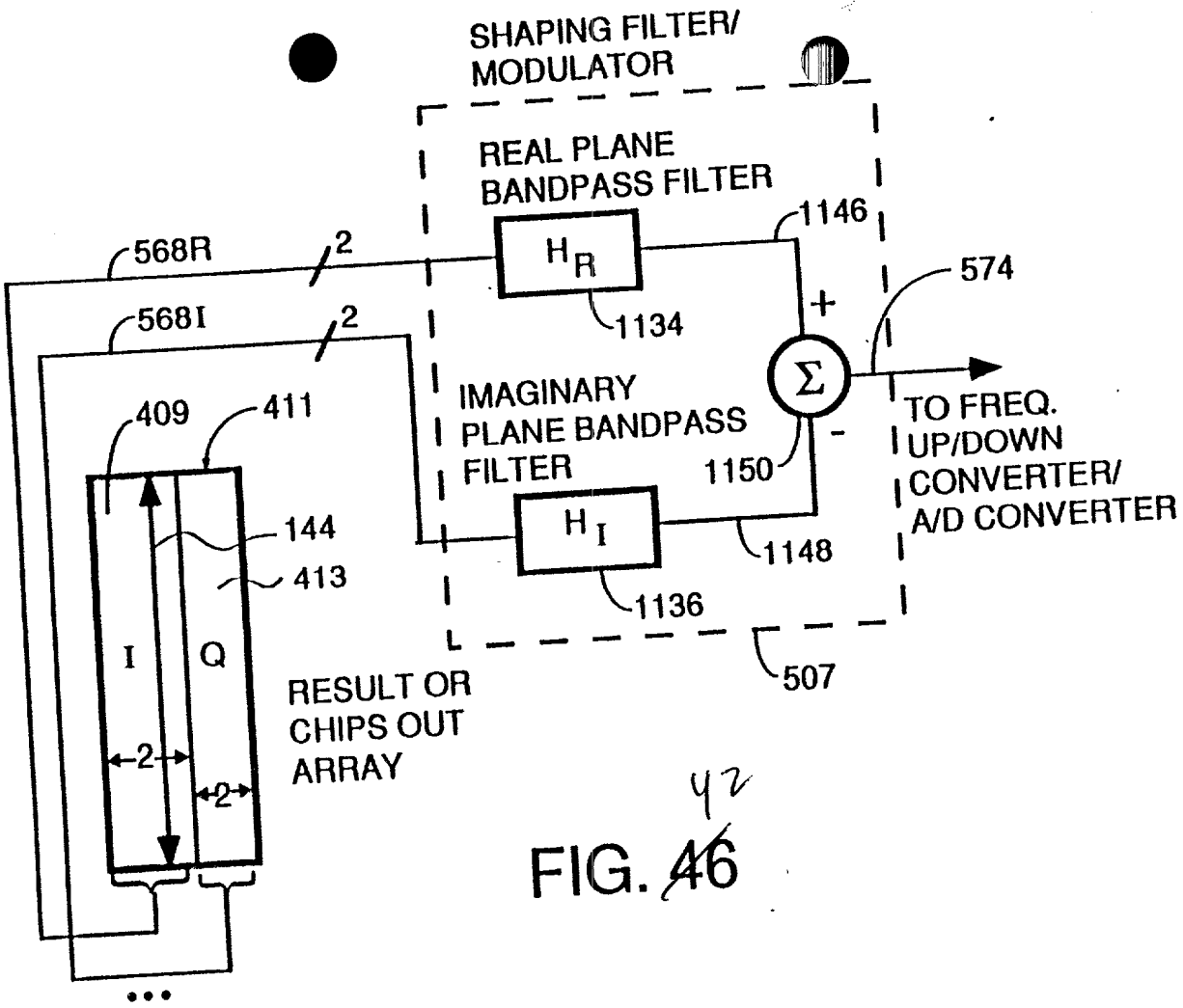
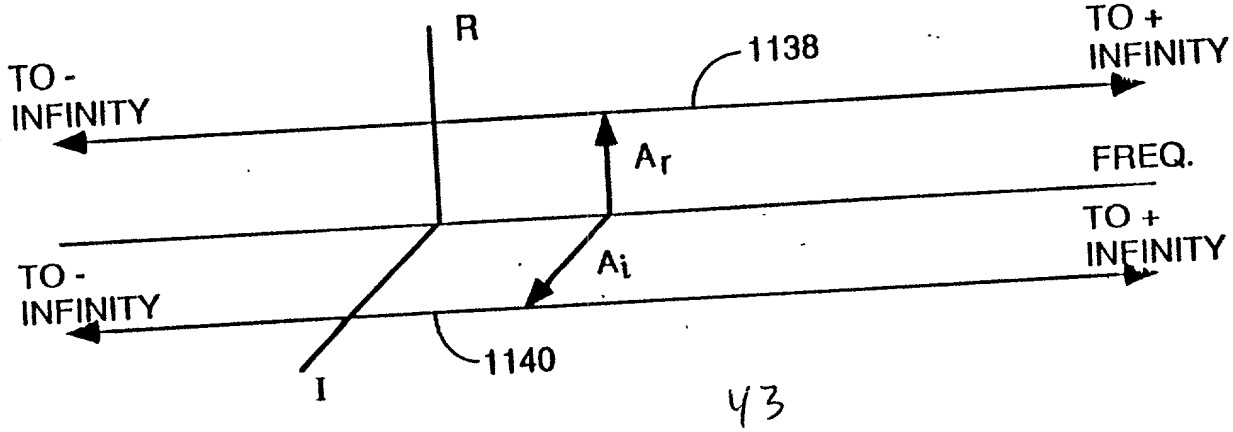


FIG. 28D



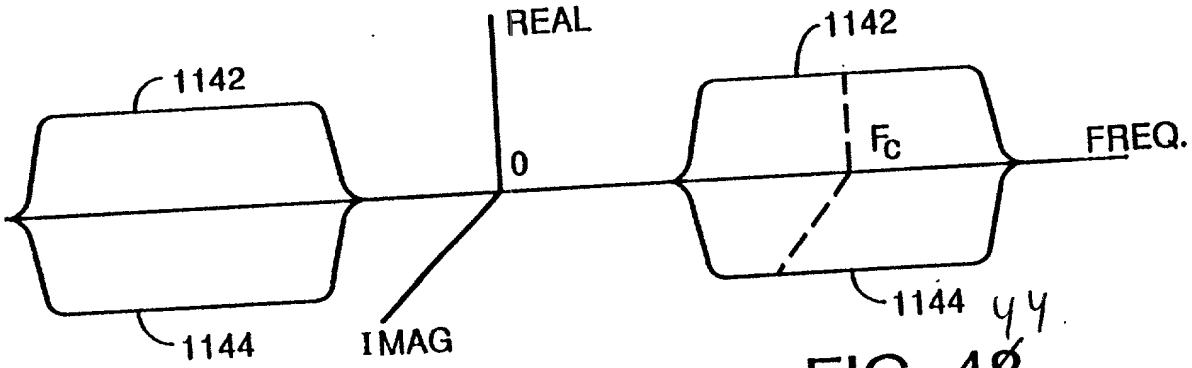
42

FIG. 46



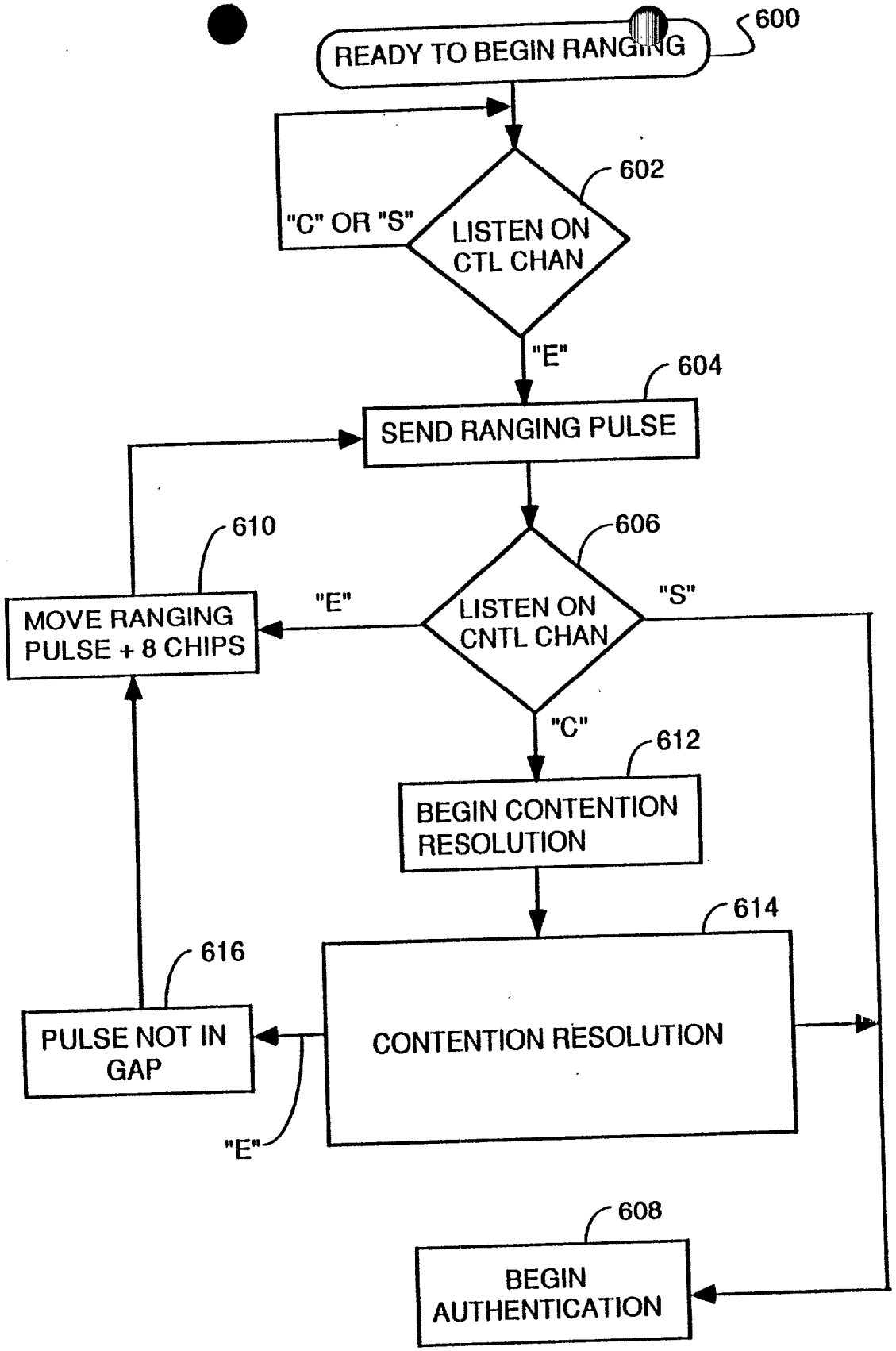
43

FIG. 47



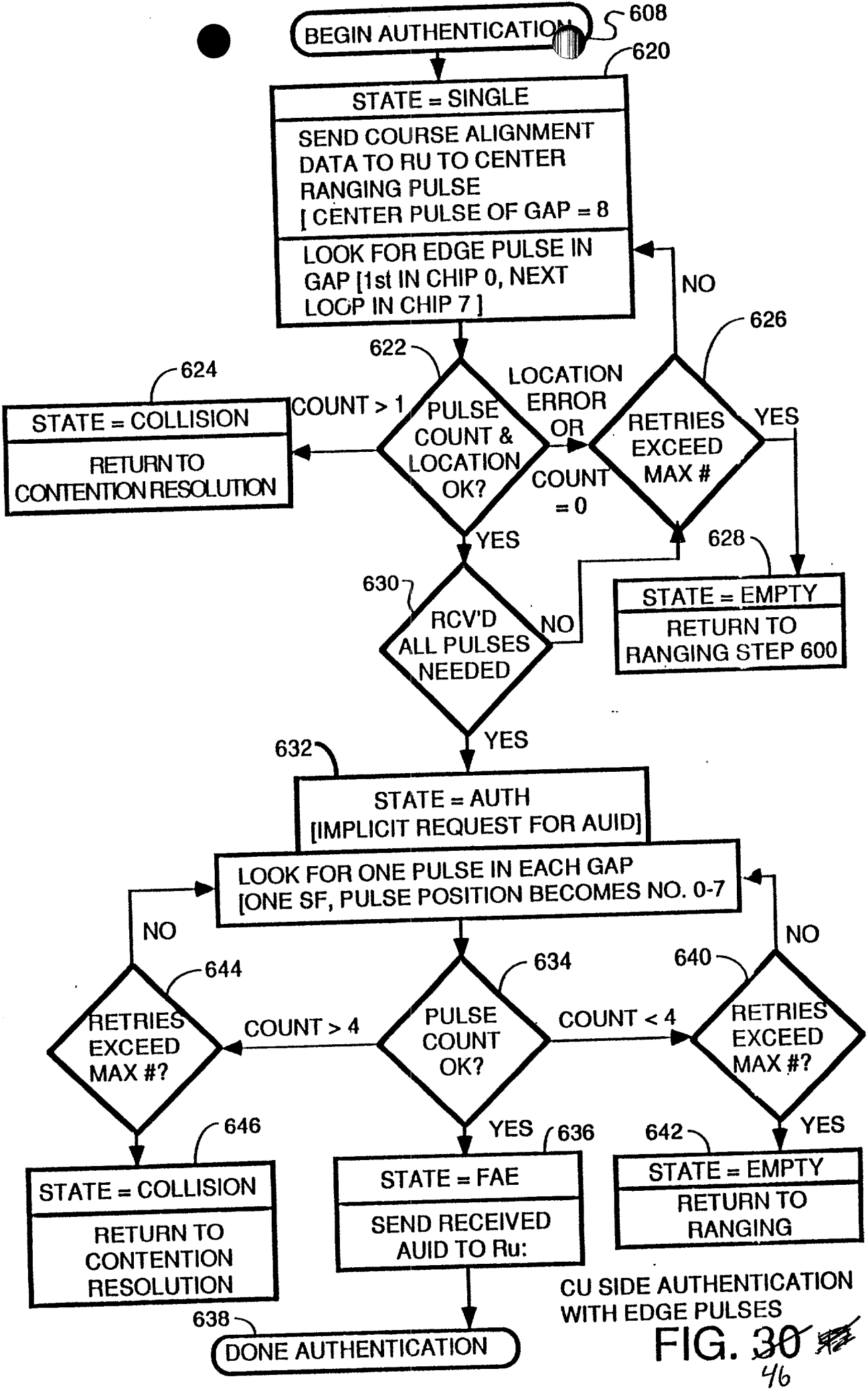
44

FIG. 48



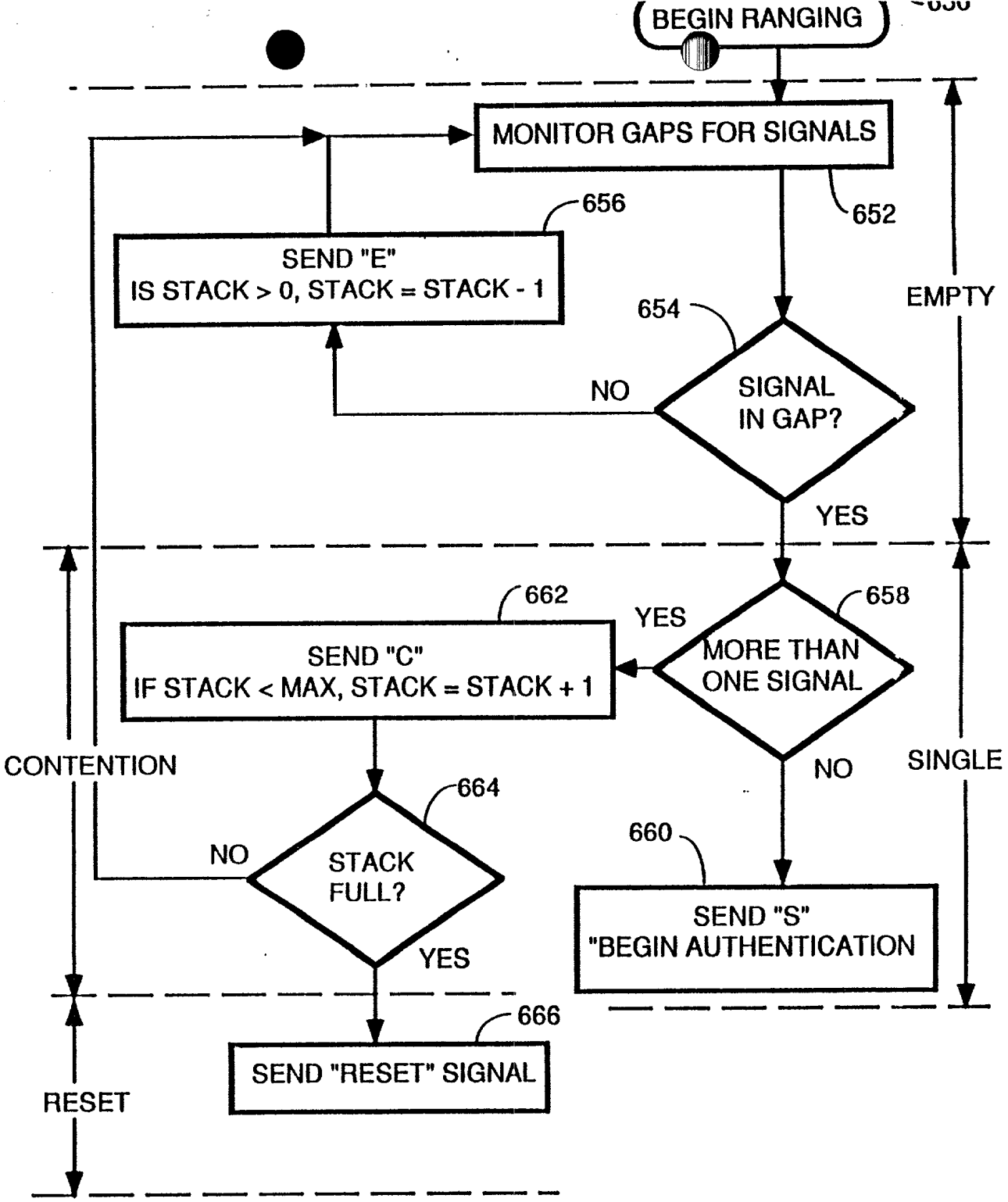
RU RANGING

FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30

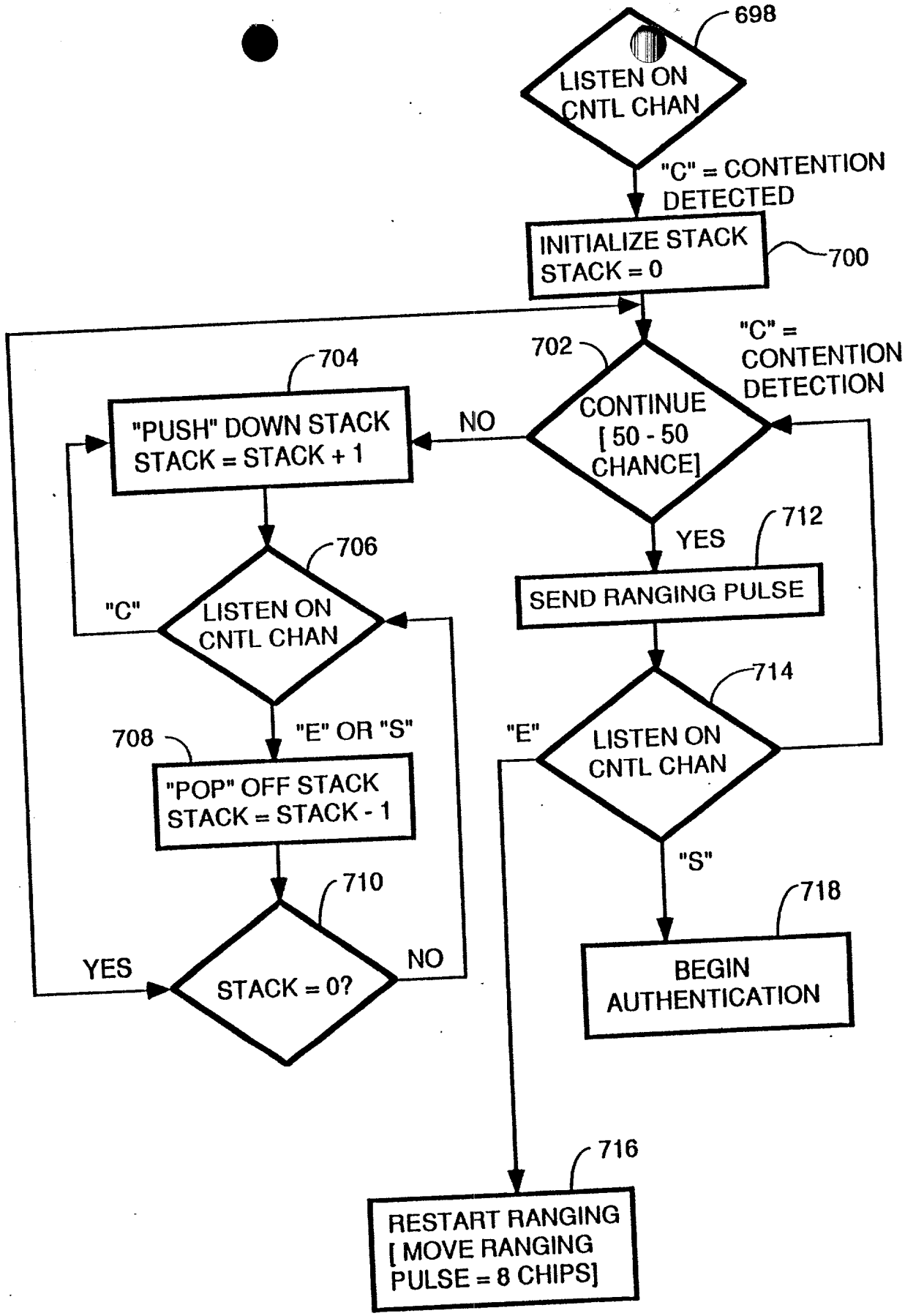


CU RANGING & CONTENTION RESOLUTION

~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

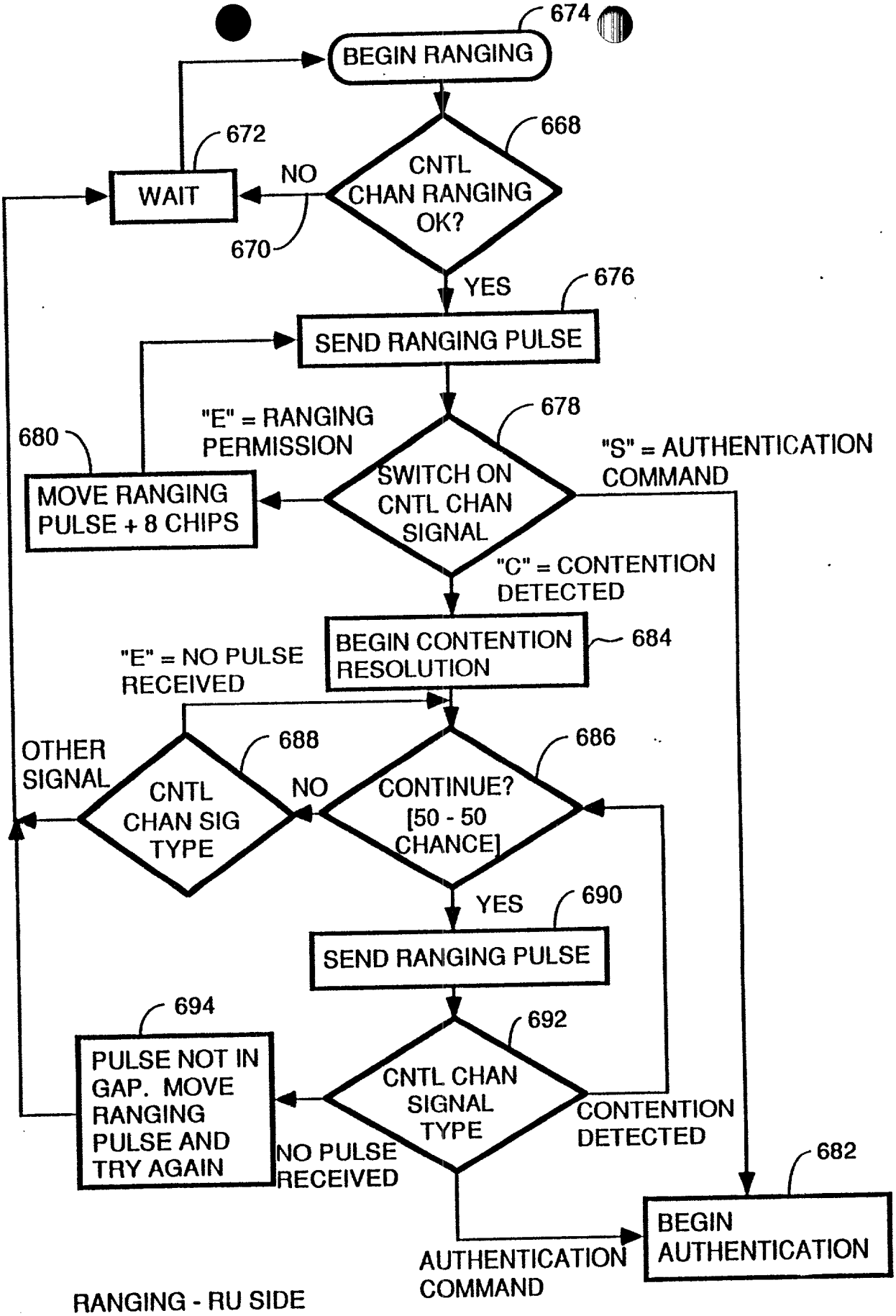
FIG. 31

47



CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. 33



RANGING - RU SIDE BINARY TREE ALGORITHM

FIG. 32

50

49

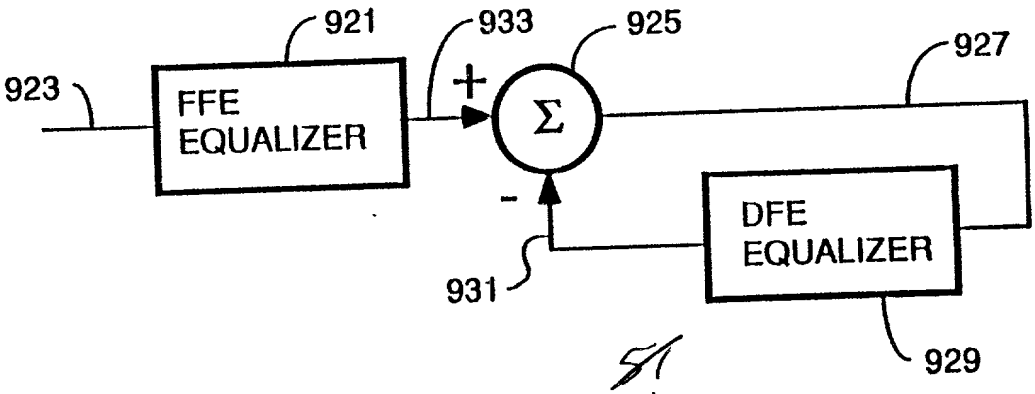


FIG. 37

50

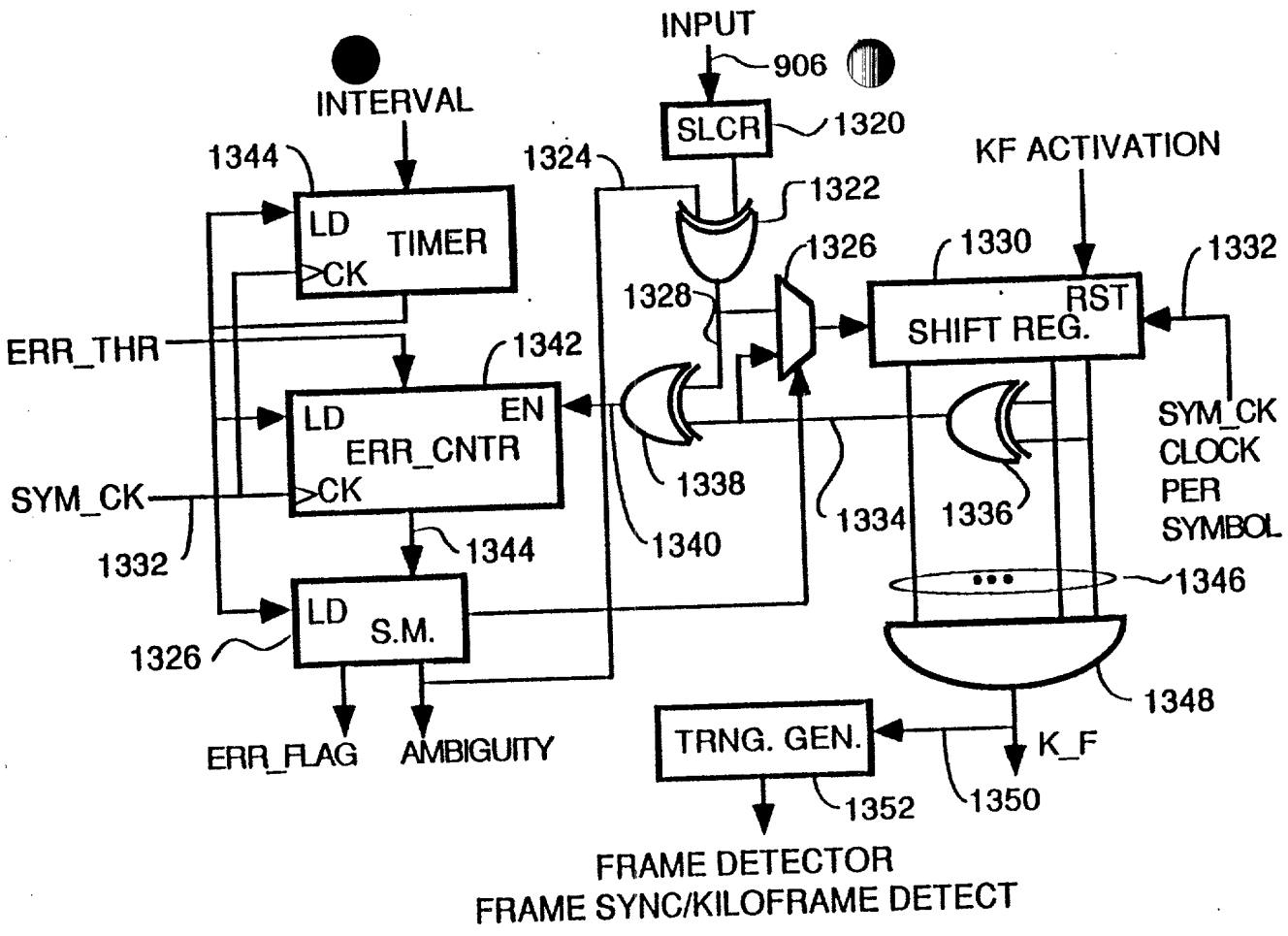
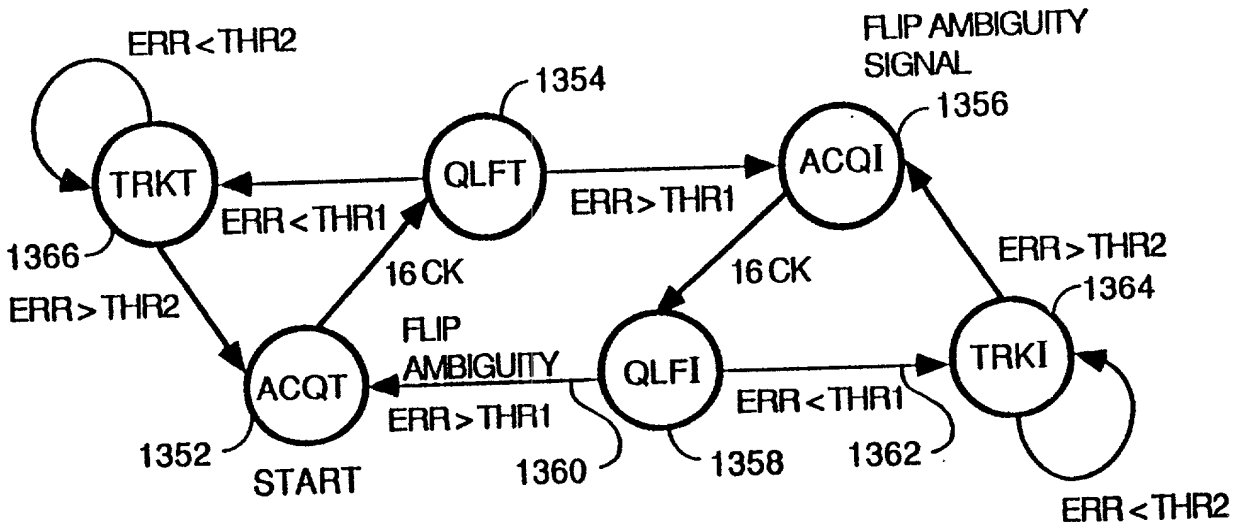


FIG. 52

51



STATE MACHINE

FIG. 53

52

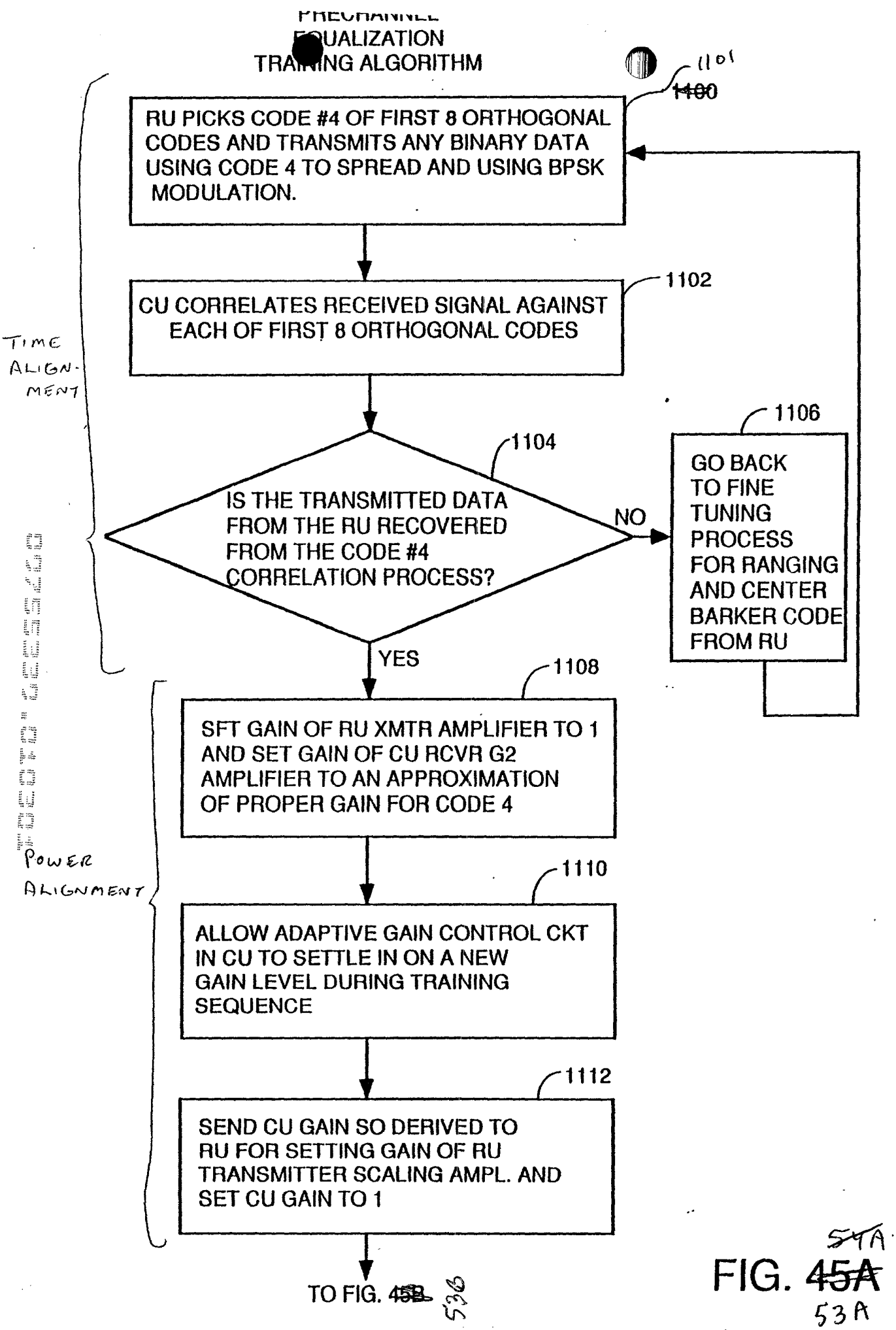

PRECHANNEL EQUALIZATION TRAINING ALGORITHM
1101
1100
RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.
1102
CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES
TIME ALIGN-MENT
1104
IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?
NO
1106
GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU
YES
1108
SFT GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4
POWER ALIGNMENT
1110
ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE
1112
SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1
TO FIG. 45B
53B

FIG. 45A
53A

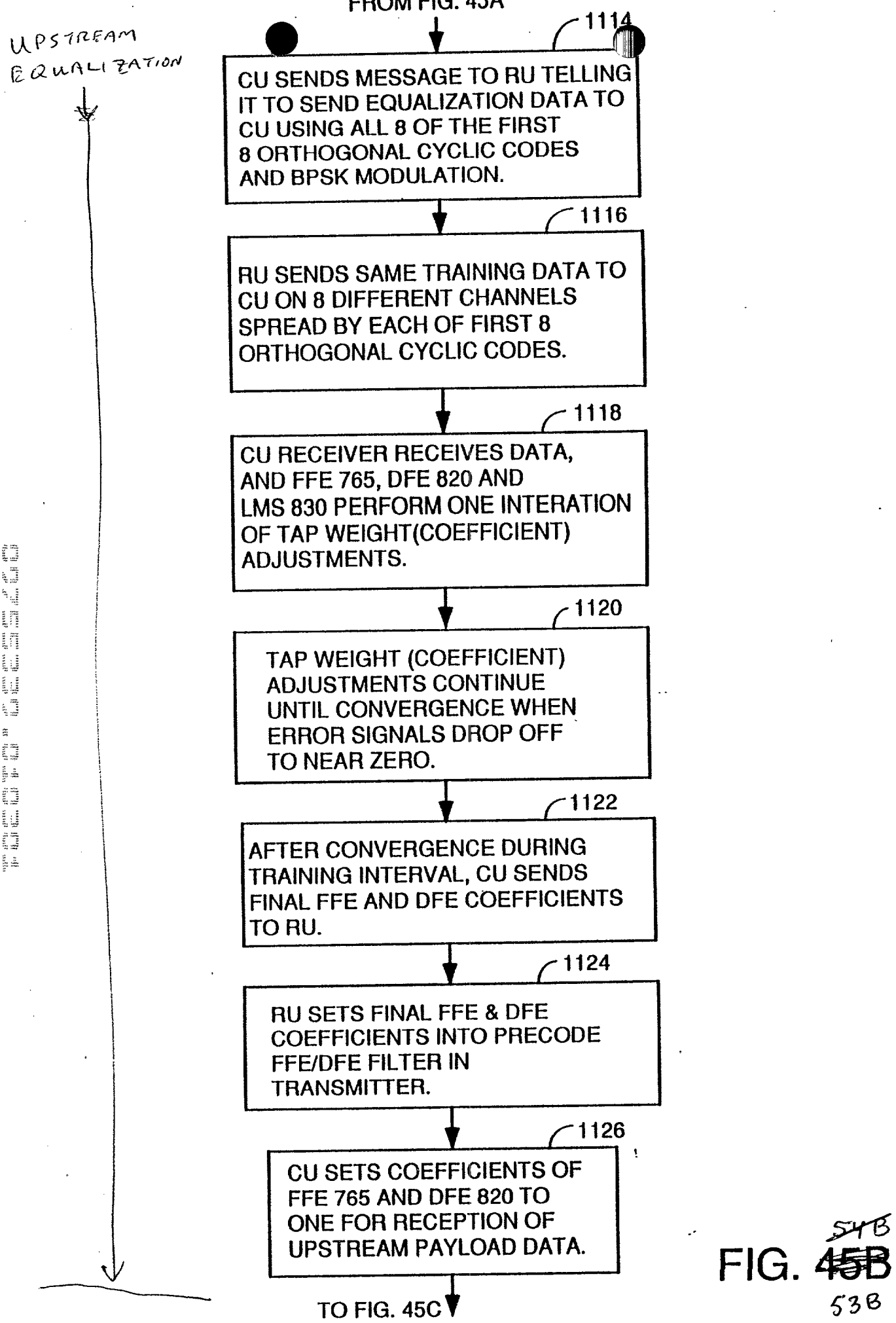


FIG. ~~45B~~ 54B

53B

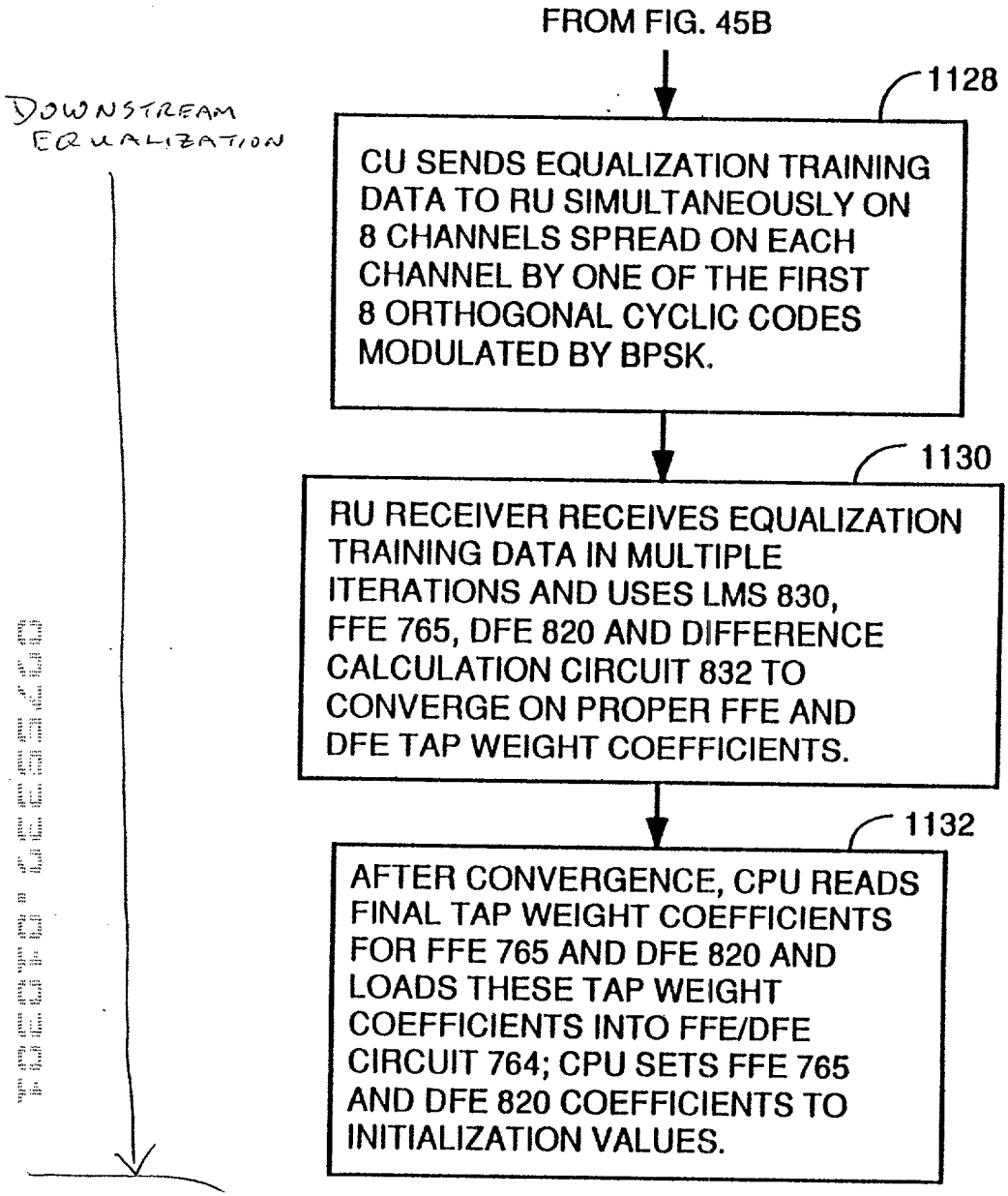


FIG. ~~45C~~ 54C 53C

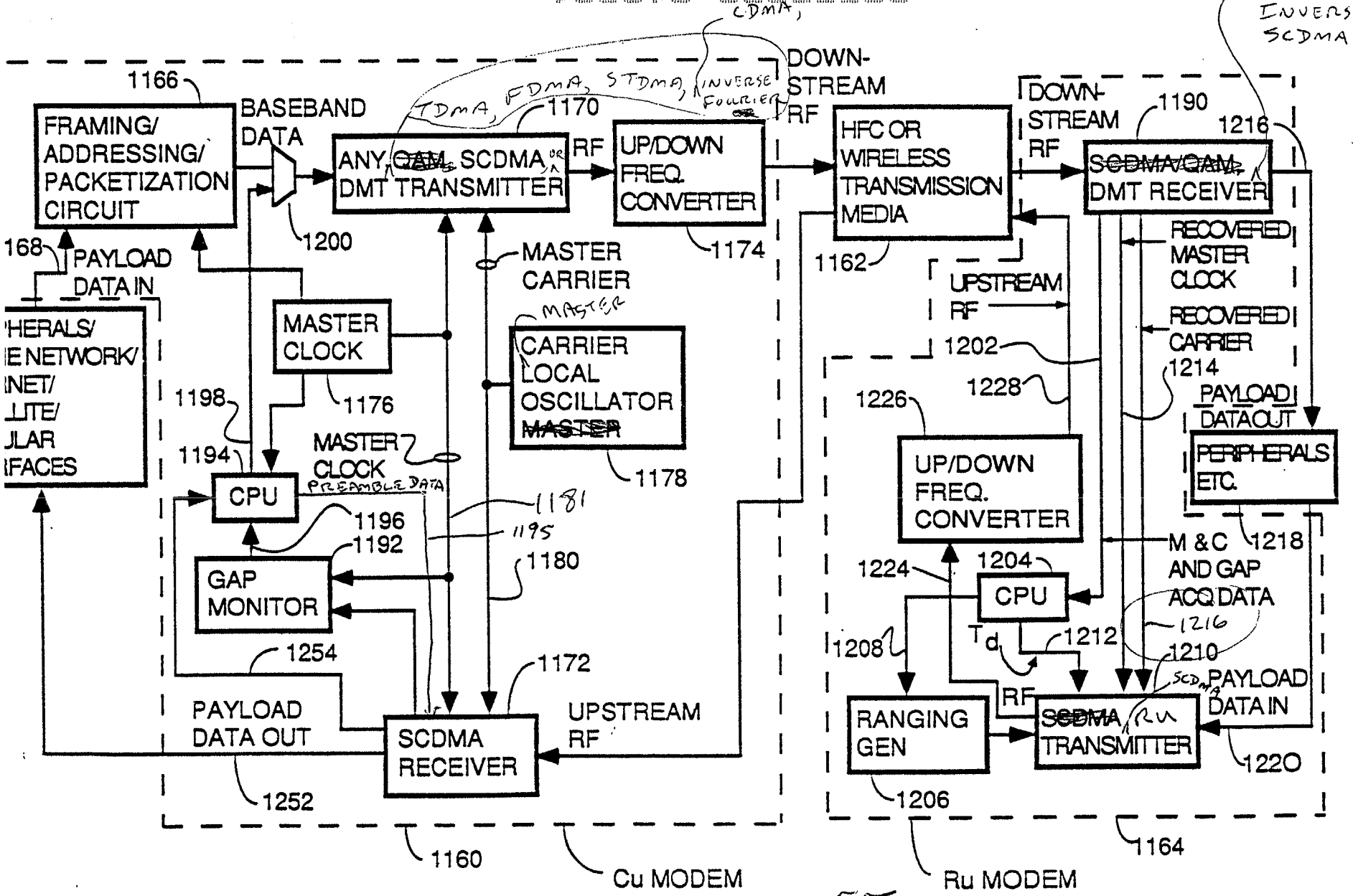
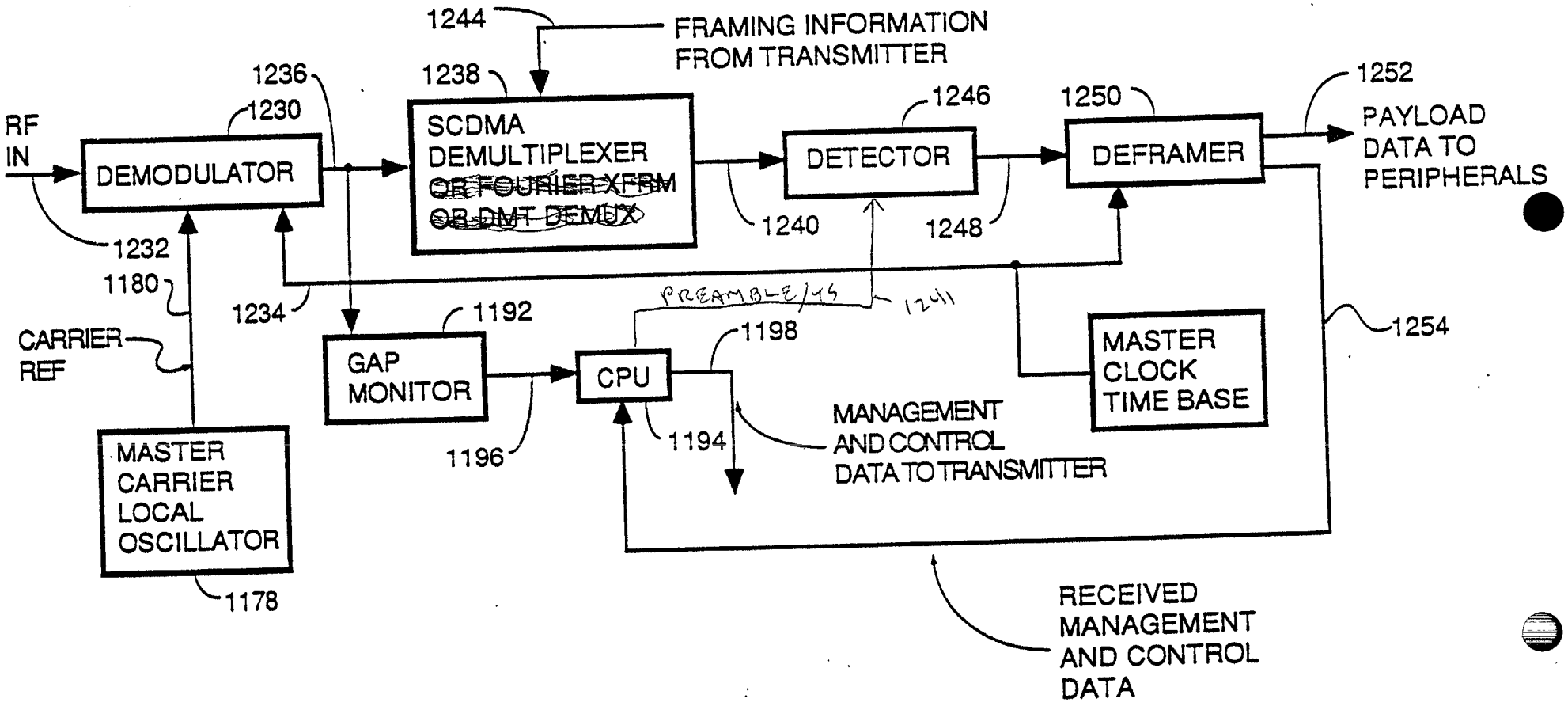

1166
FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
BASEBAND DATA
1200
168
PAYLOAD DATA IN
HERALS/ E NETWORK/ INET/ LITE/ JLAR IFACES
MASTER CLOCK
1176
1198
1194
CPU
MASTER CLOCK
PREAMBLE DATA
1196
1192
GAP MONITOR
1254
PAYLOAD DATA OUT
1252
1160
Cu MODEM
1170
ANY SCDMA DMT TRANSMITTER
RF
UP/DOWN FREQ. CONVERTER
1174
MASTER CARRIER
CARRIER LOCAL OSCILLATOR
1178
1181
1195
1180
1172
SCDMA RECEIVER
UPSTREAM RF
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
1162
UPSTREAM RF
1202
1228
1226
UP/DOWN FREQ. CONVERTER
1224
1204
CPU
1208
Td
1212
RANGING GEN
1206
RF
SCDMA TRANSMITTER
1220
1164
Ru MODEM
DOWN-STREAM RF
1190
1216
SCDMA DMT RECEIVER
RECOVERED MASTER CLOCK
RECOVERED CARRIER
1214
PAYLOAD DATA OUT
PERIPHERALS ETC.
1218
M & C AND GAP ACQ DATA
1216
1210
SCDMA PAYLOAD DATA IN
TDMA, FDMA, STDMA, INVERSE FOURIER
CDMA,
TDMA, STDMA, F
INVERSE FOURIE
SCDMA, CDMA OR

FIG. 49

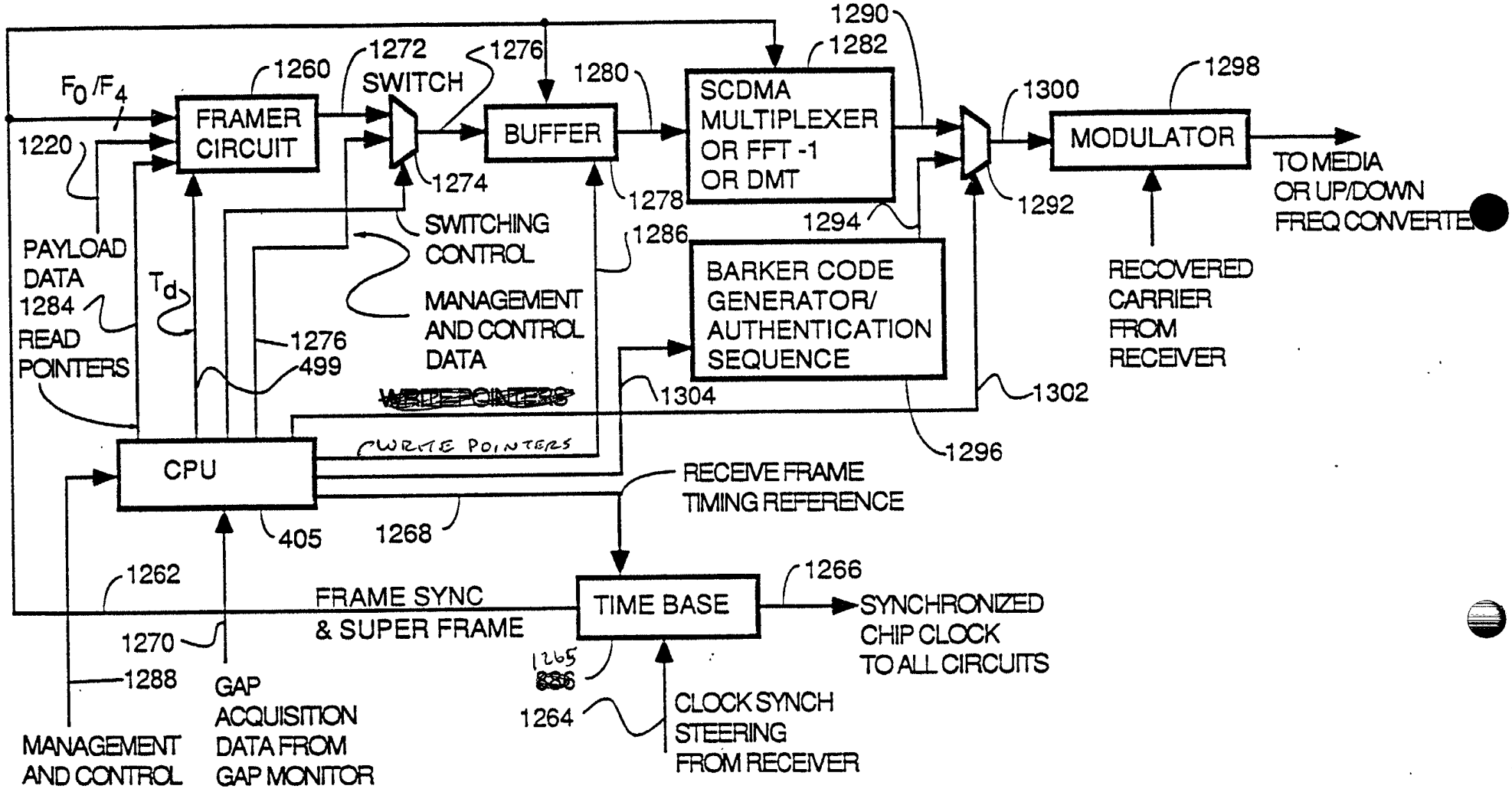
54



SIMPLE Cu SPREAD SPECTRUM RECEIVER

FIG. ~~50~~ 56

55

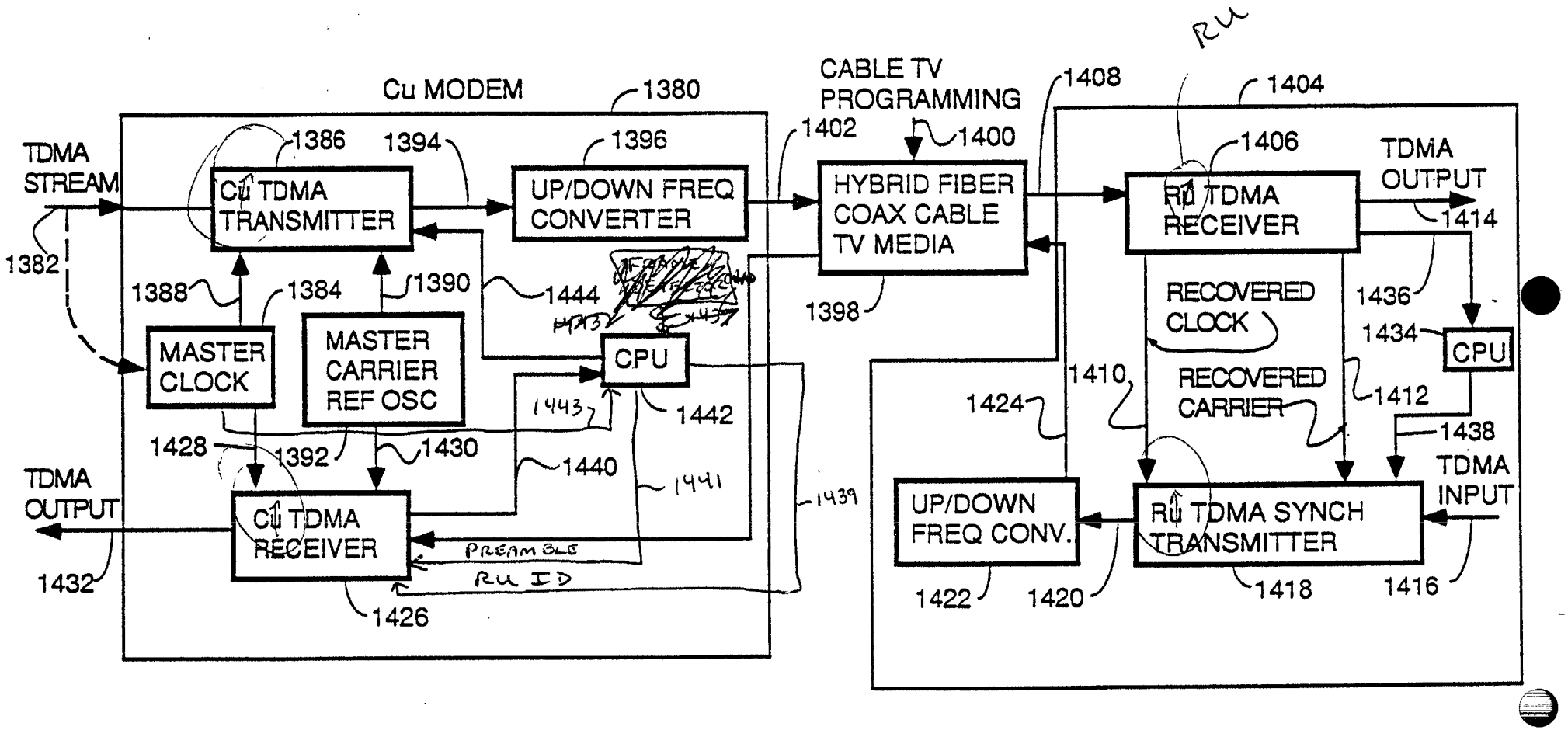


SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. 5~~1~~

~~5~~7

56



SYNCHRONOUS TDMA SYSTEM

FIG. 54

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OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

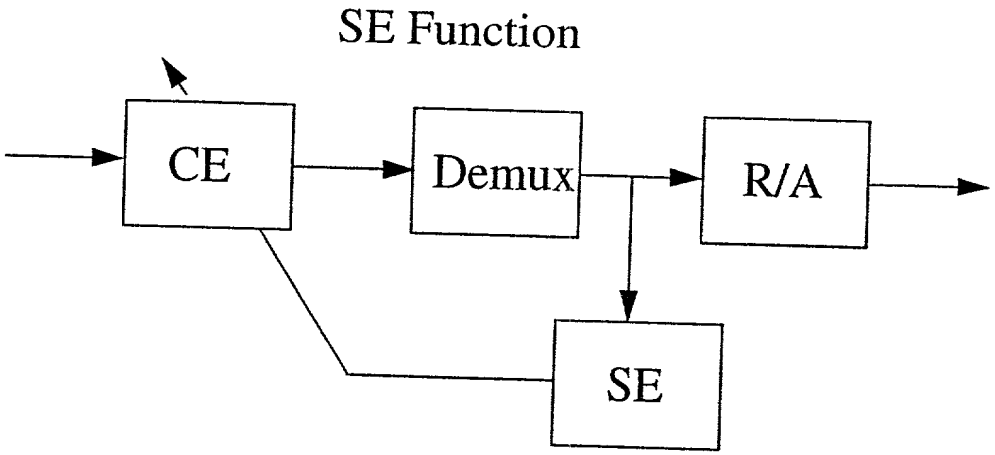
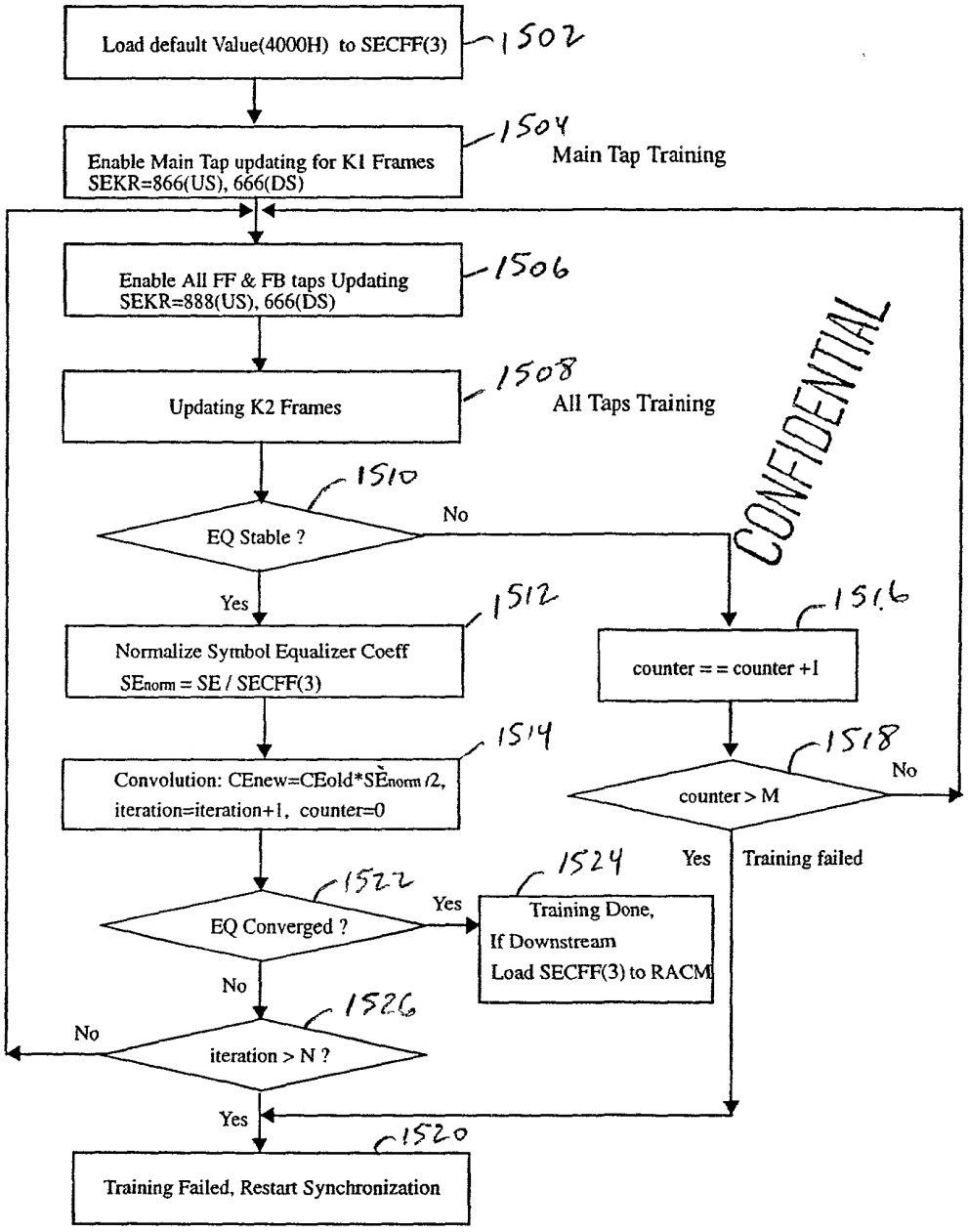


FIG. 59

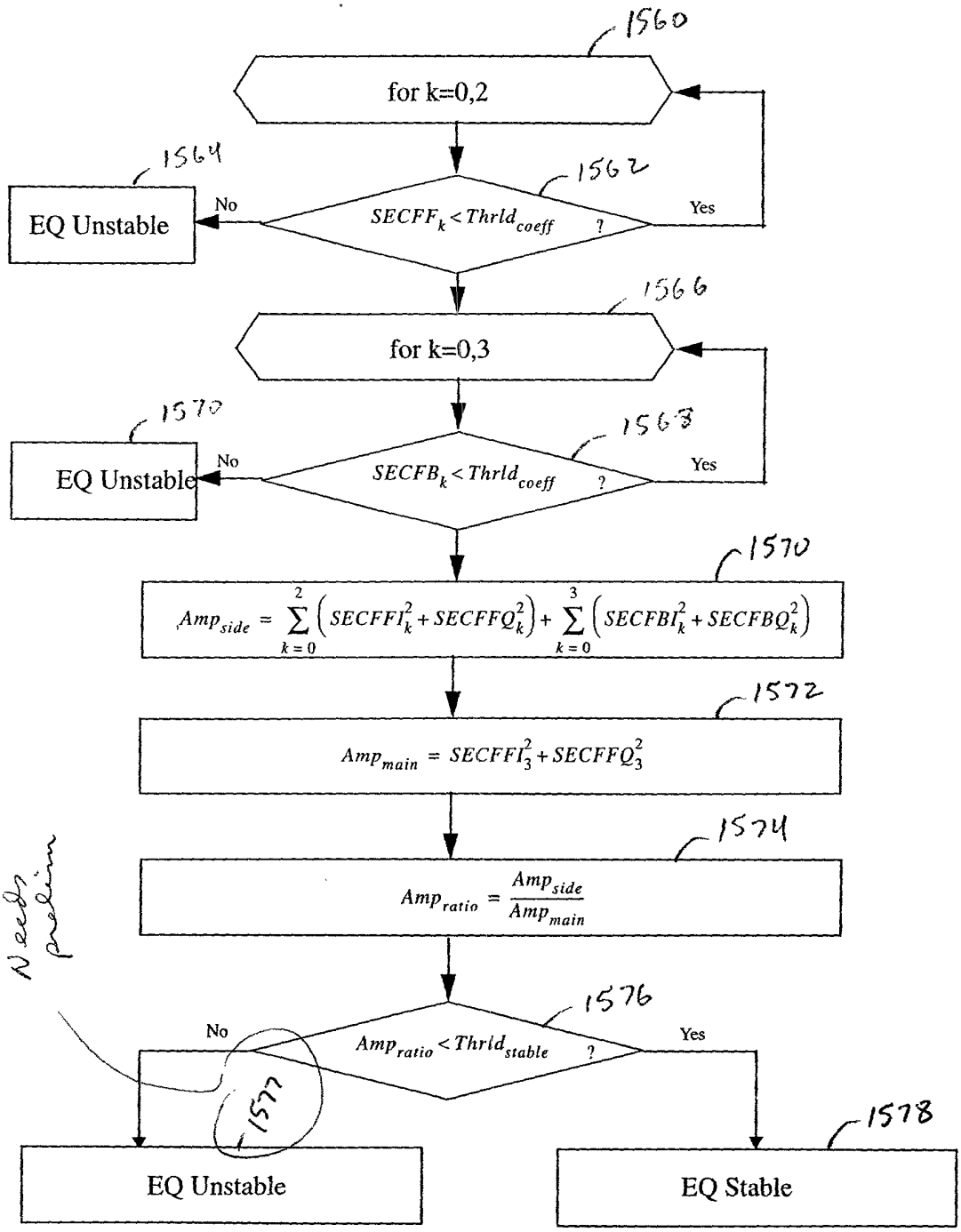
Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

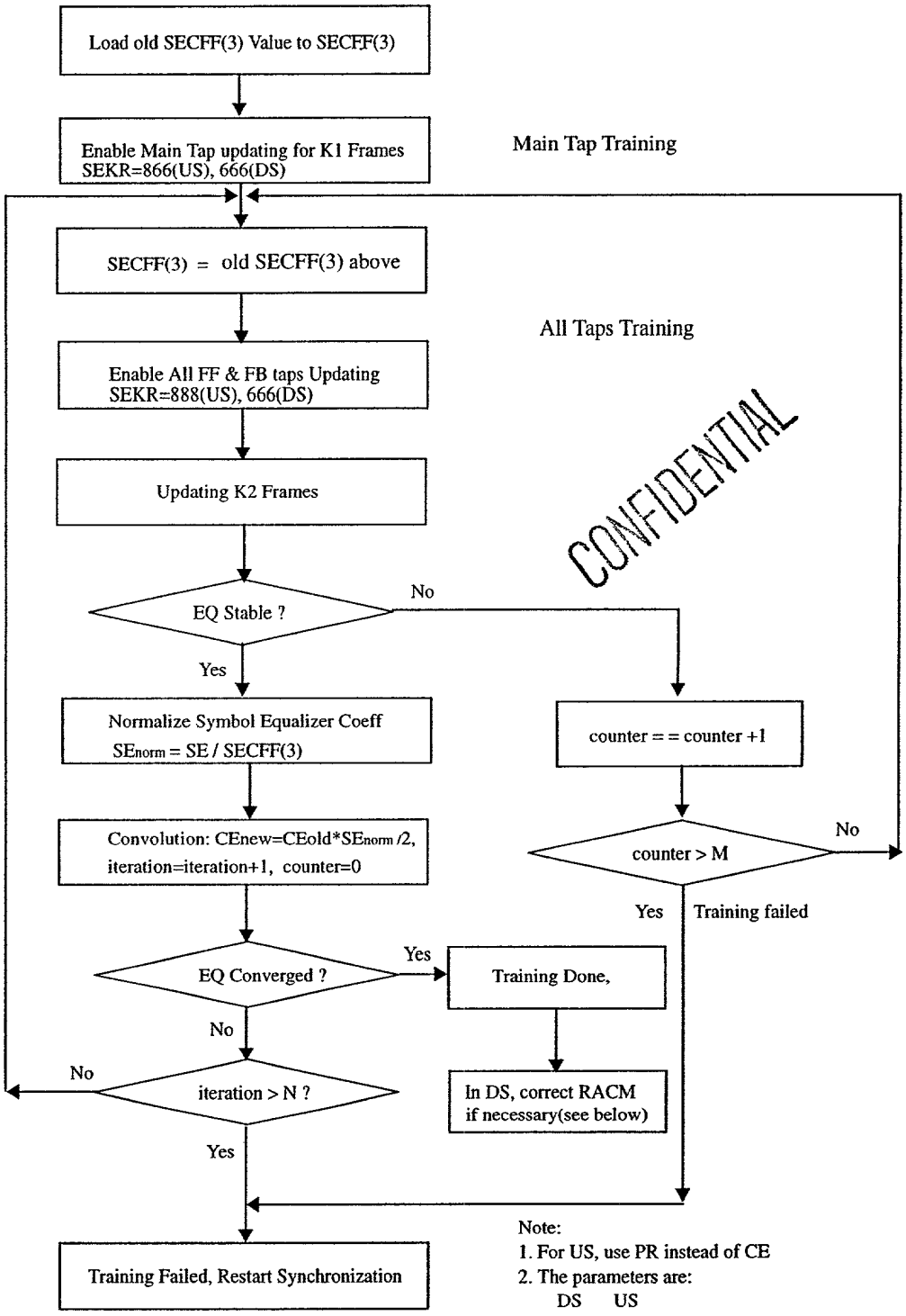
EQ Stability Check



Note: $Thrld_{coeff} = 7F00H$ $Thrld_{stable} = 10^{-3}$

FIG. 61

Periodic 2-Step Training Algorithm

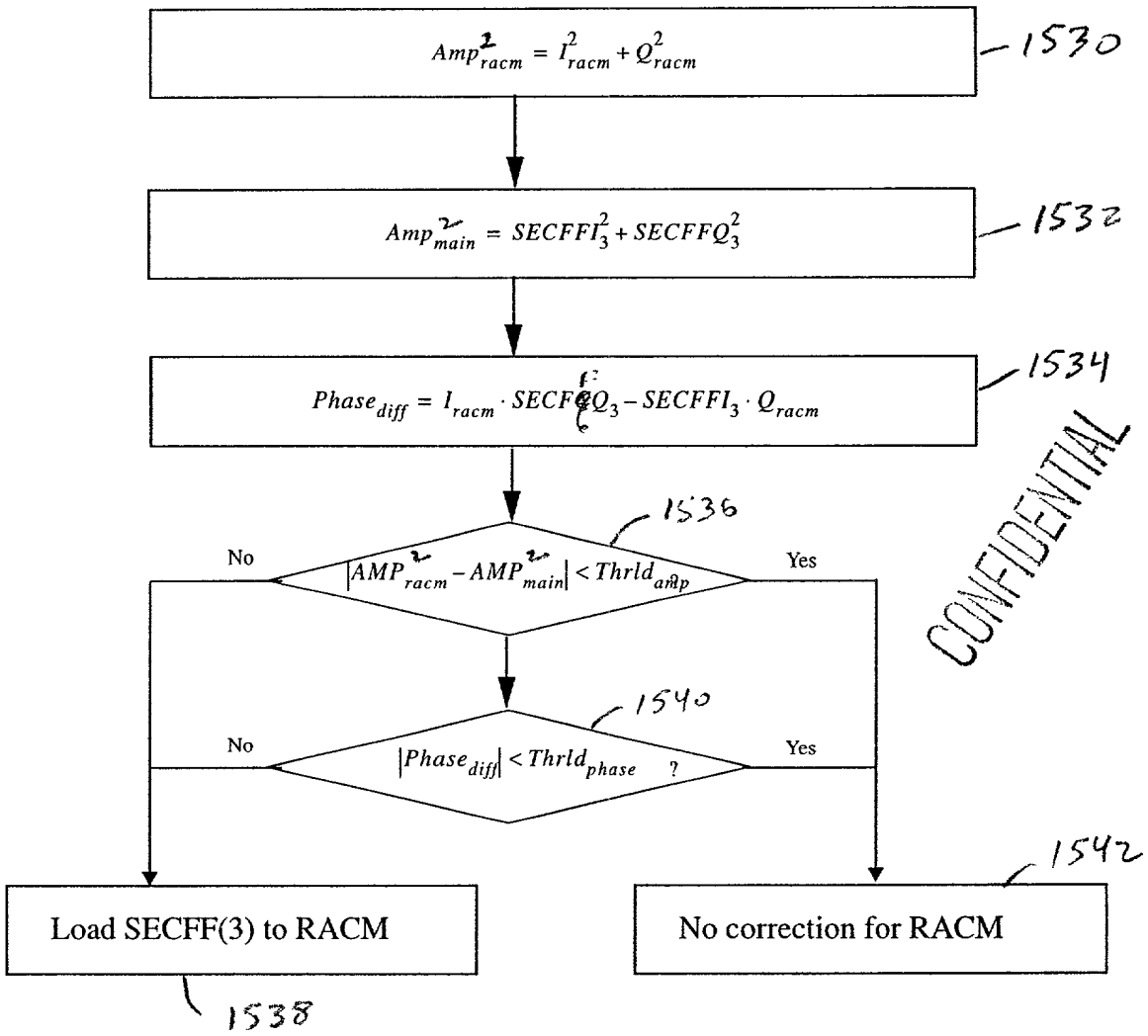


Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



CONFIDENTIAL

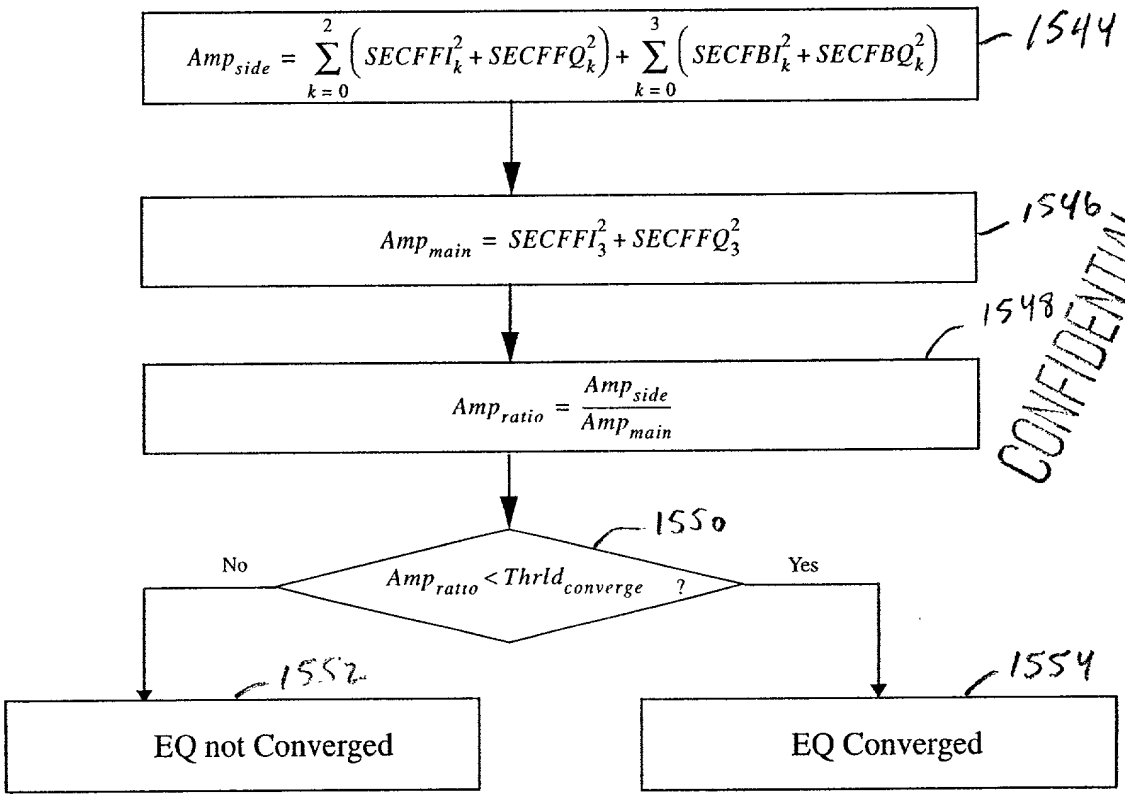
Note: $Thrld_{amp} = TBD$

$Thrld_{phase} = TBD$

RATIONAL AMPLIFIER CORRECTION

FIG. 63.

EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart

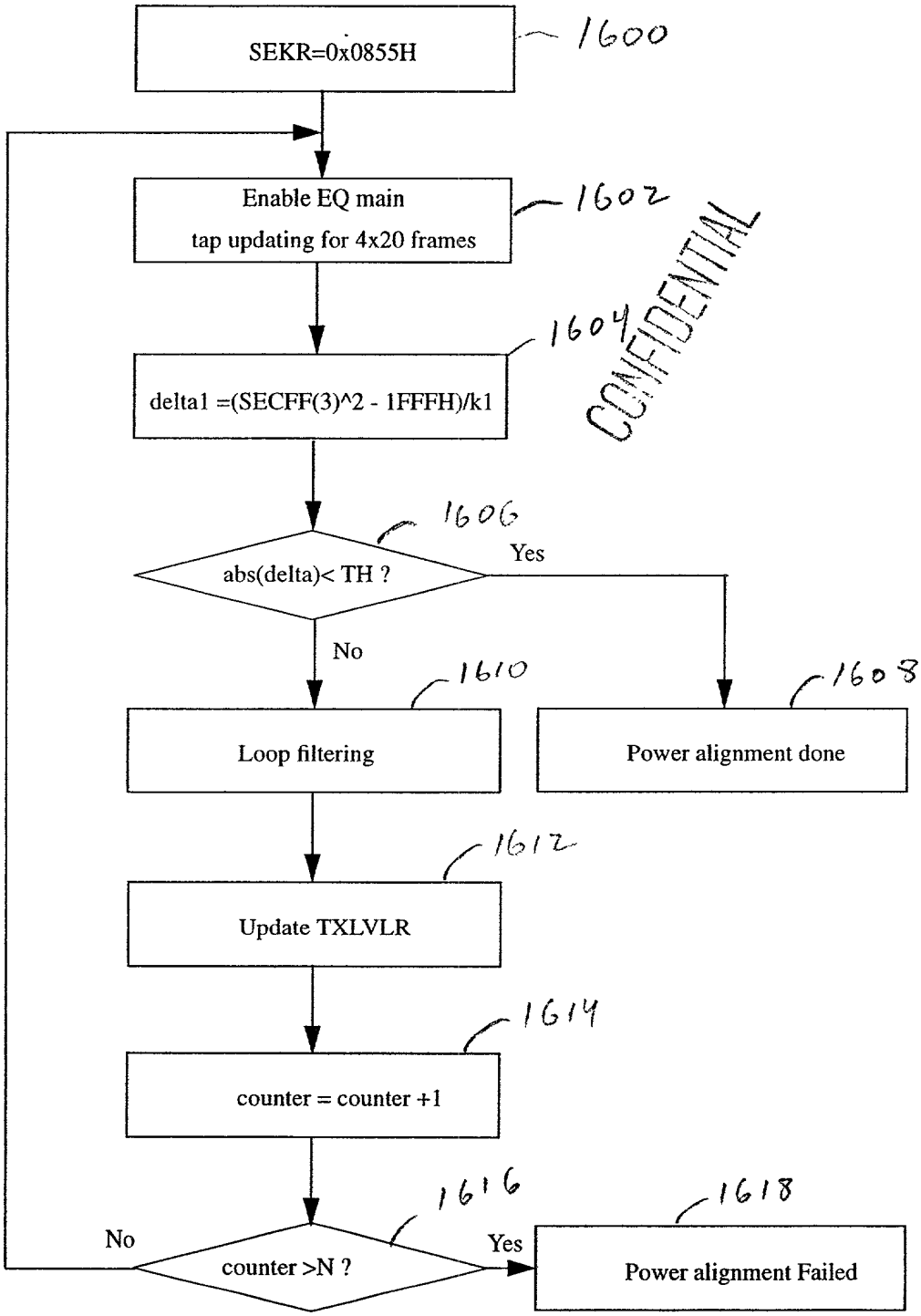


FIG. 65

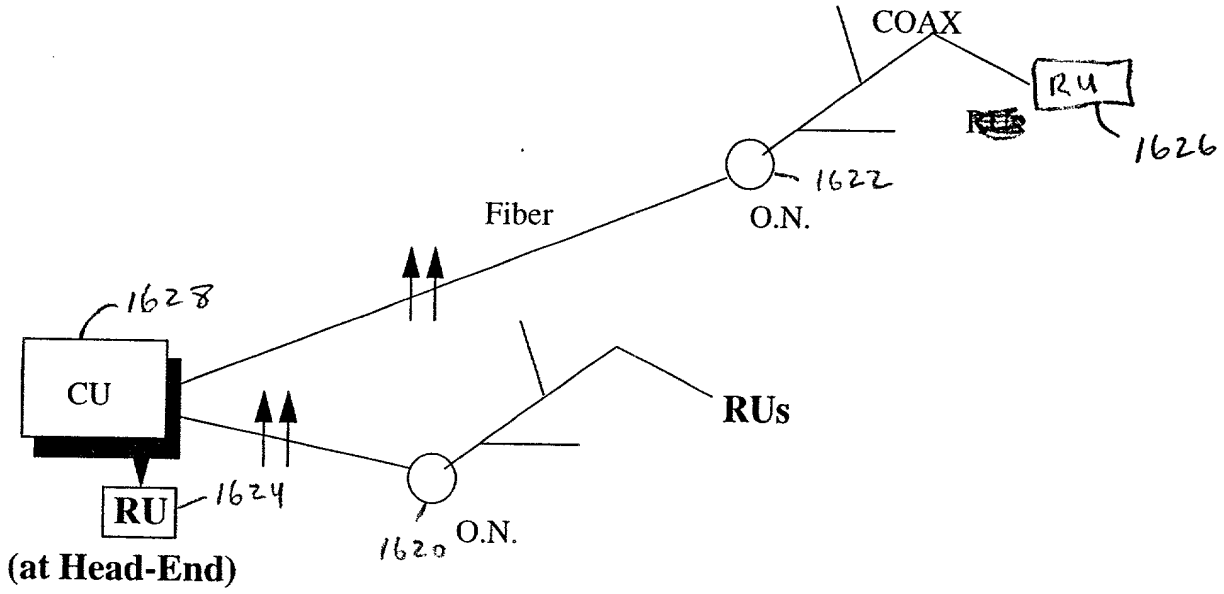
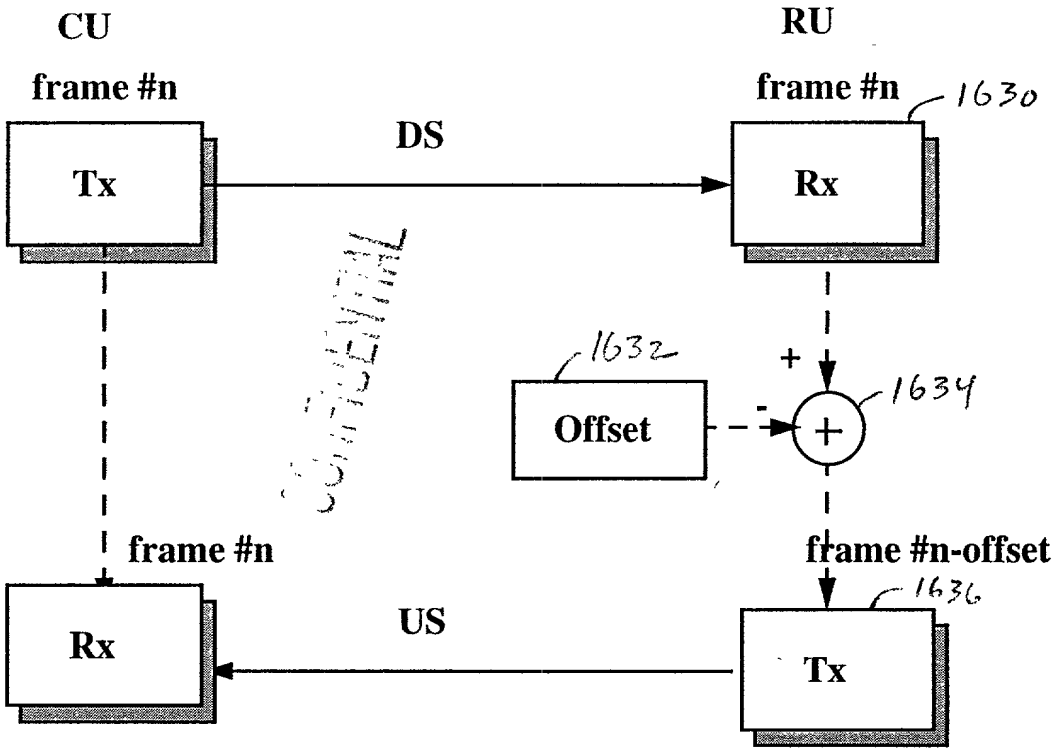


FIG. 66



Total Turn Around (TTA) in frames = Offset

FIG. 67

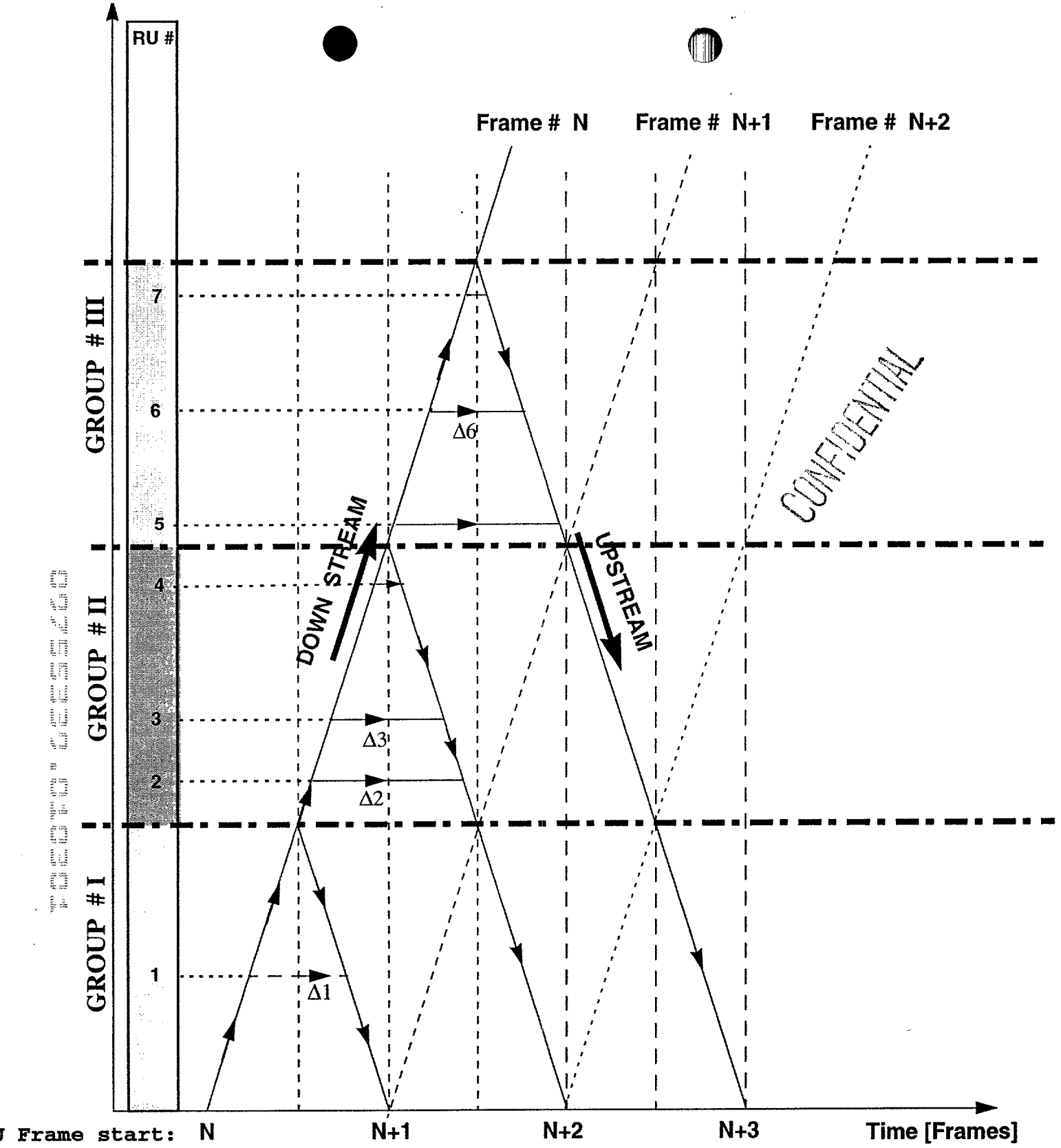


FIG. 6B

Figure 3.1: Frame start propagation along the channel

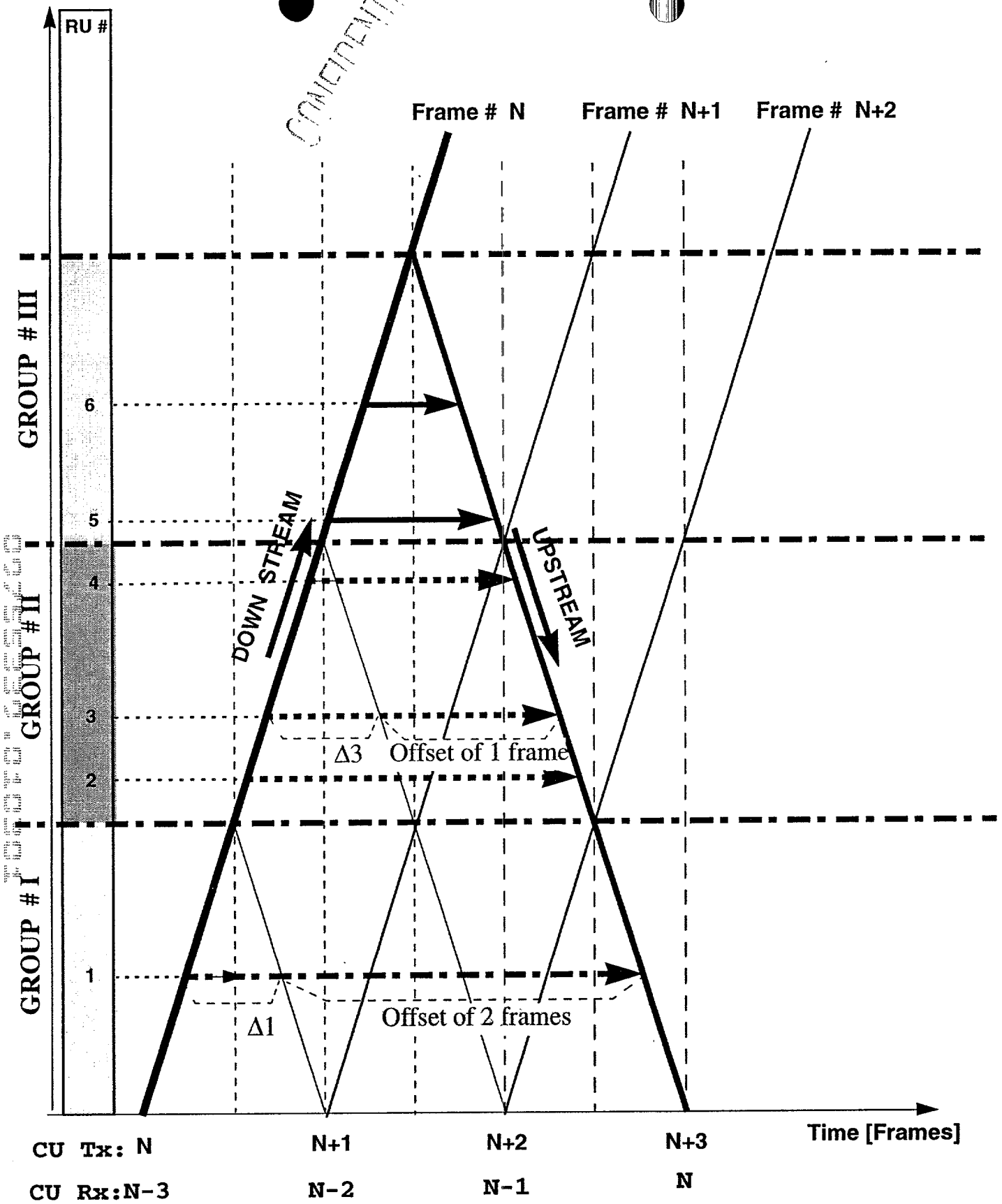


FIG. 69

Figure 3-2 Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

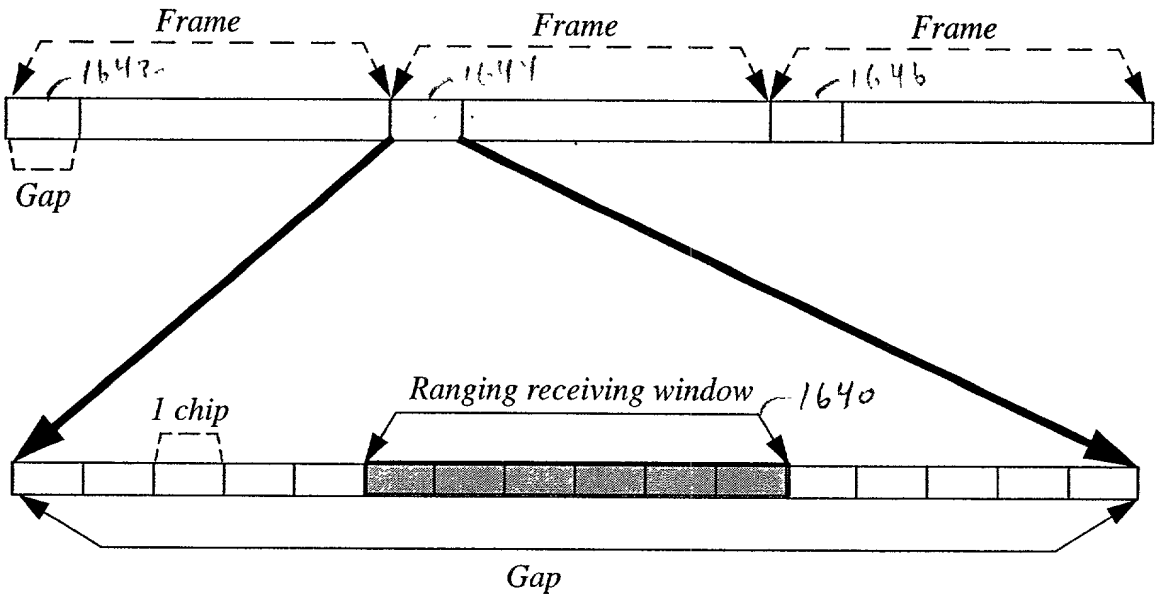

Frame
Frame
Frame
1642
1644
1646
Gap
1 chip
Ranging receiving window
1640
Gap

FIG. 70

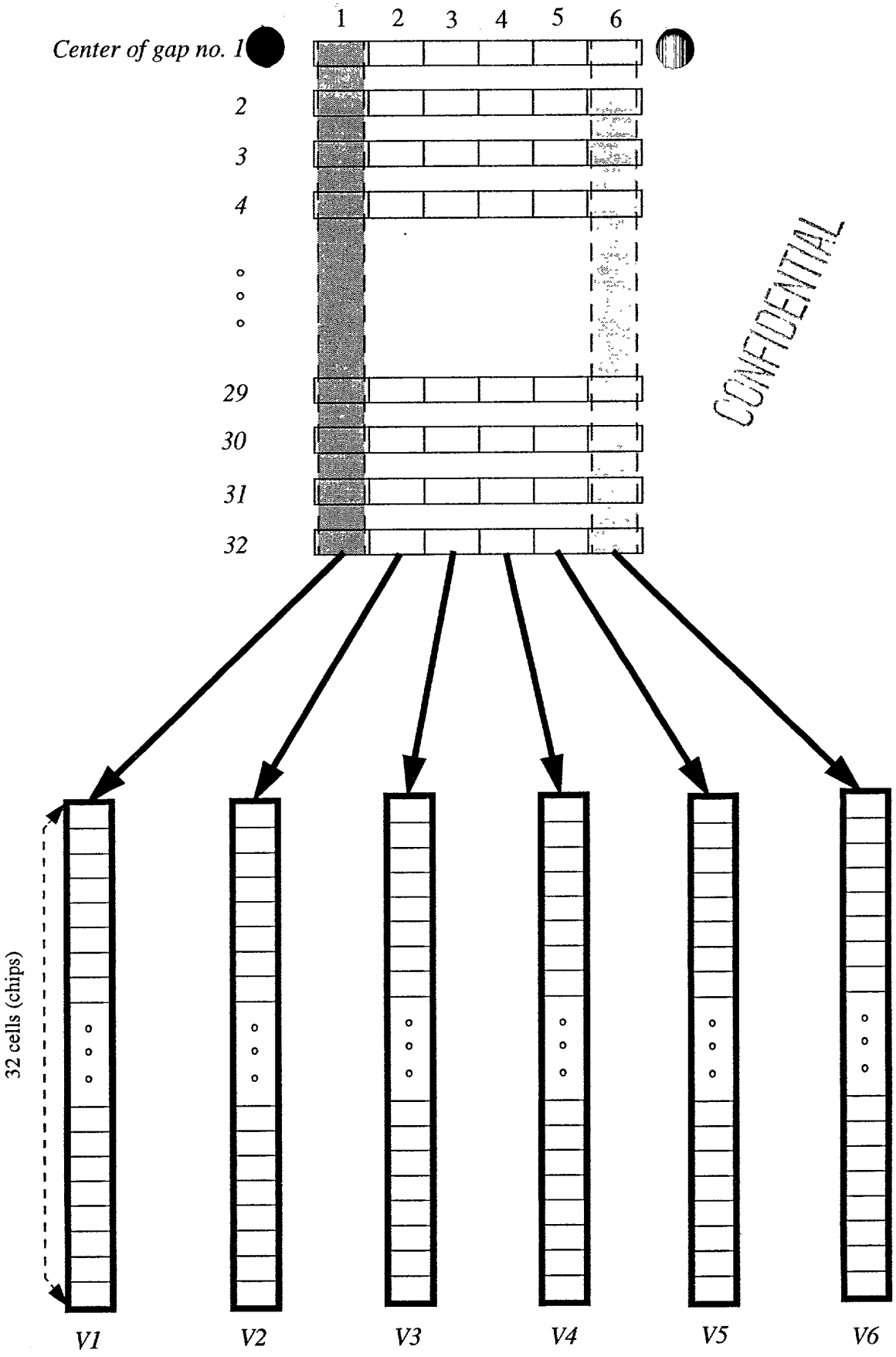


Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 7I

6

Chip\FR	1	2	3	4	5	6	7		33
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**...**	**0**
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72